

Neptune_KLS

Schematics Document

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
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Document Number

Neptune_KLS

Rev

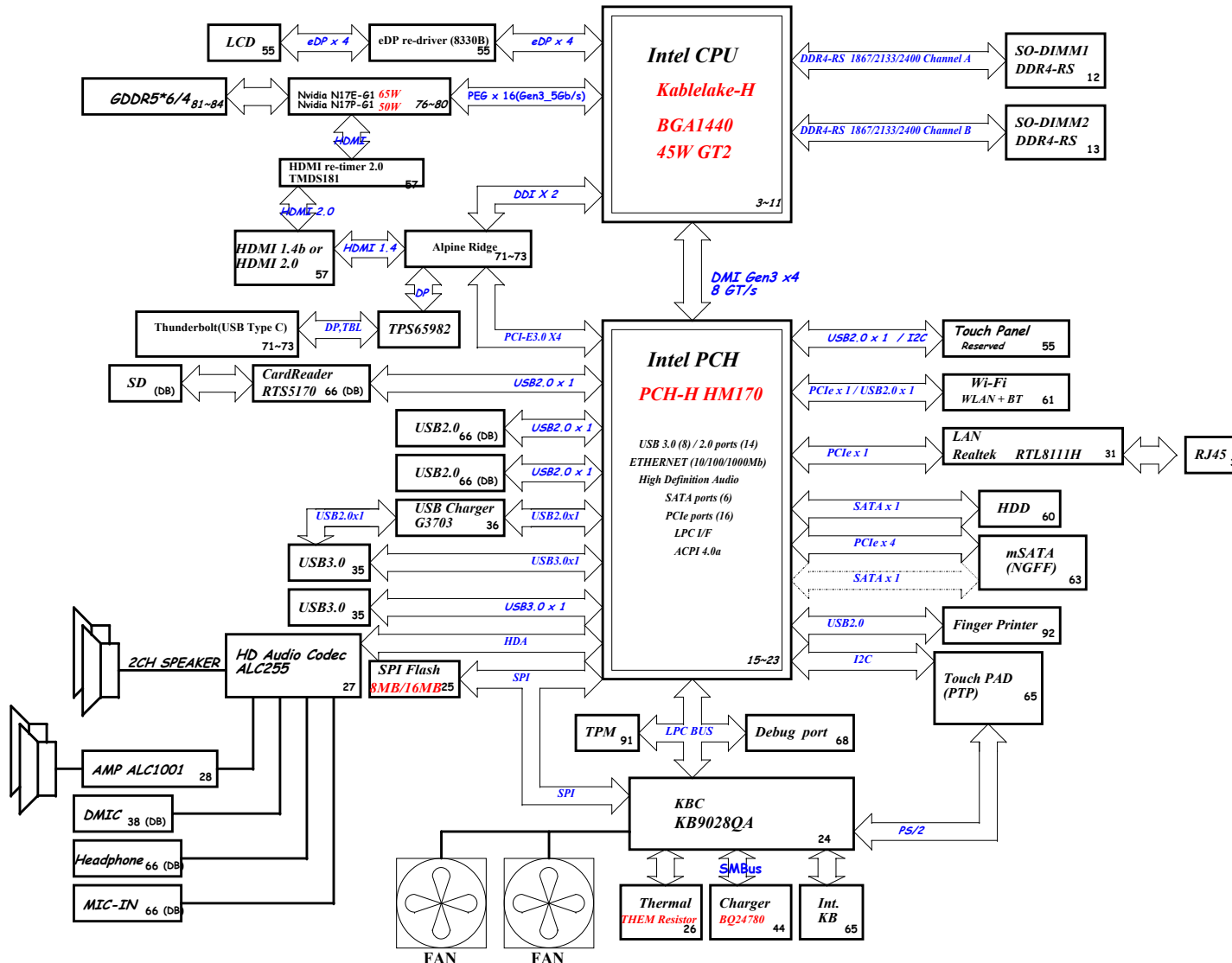
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Date: Wednesday, May 17, 2017

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Neptune_KLS Board Block Diagram

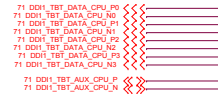
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PCB P/N : 16834
Revision : 1m



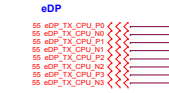
CHARGER BQ24780SRUYR 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT
SYSTEM DC/DC RT6575D 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5
CPU Core Power ISL95855HRTZ 46, 47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DDR4 power APW8861QBI-TRG 51	
INPUTS	OUTPUTS
DCBATOUT	1D2V_S3 2D5V_S3 0D6V_S0
1D0V_S5 RT8231AGW 52	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5
CPU 1D8V_S0 RT9025 53	
INPUTS	OUTPUTS
3D3V_S5 5V_S5	1D5V_S0
Switches 40	
INPUTS	OUTPUTS
5V_S0 3D3V_S5 1D0V_S5	3D3V_S0 0D95V_VCCIO 1V_VCCST

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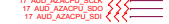
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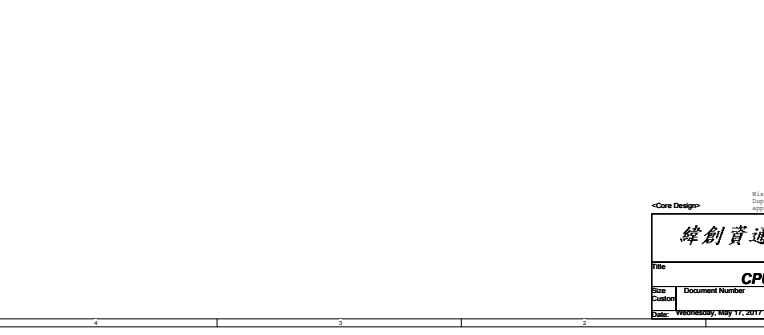
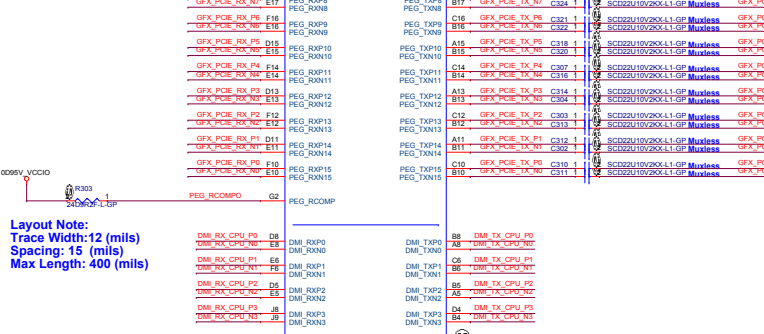
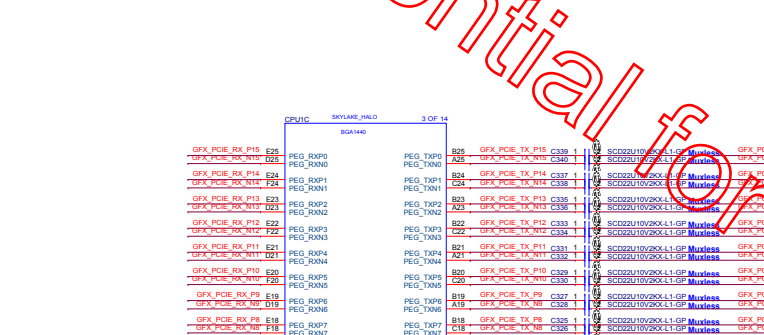
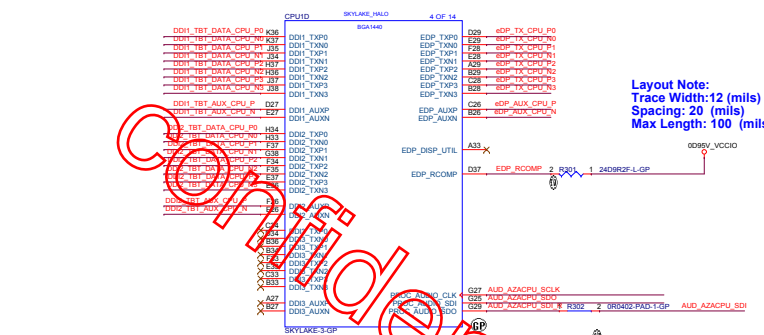
DD2



Soc AUD



PEG



Layout Note:
Trace Width: 12 (mils)
Spacing: 20 (mils)
Max Length: 100 (mils)

Layout Note:
Trace Width: 12 (mils)
Spacing: 15 (mils)
Max Length: 400 (mils)

12 M_A_DQ00
12 M_A_DQ01
12 M_A_DQ02
12 M_A_DQ03
12 M_A_DQ04
12 M_A_DQ05
12 M_A_DQ06
12 M_A_DQ07
12 M_A_DQ08
12 M_A_DQ09
12 M_A_DQ10
12 M_A_DQ11
12 M_A_DQ12
12 M_A_DQ13
12 M_A_DQ14
12 M_A_DQ15
12 M_A_DQ16
12 M_A_DQ17
12 M_A_DQ18
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12 M_A_DQ31
12 M_A_DQ32
12 M_A_DQ33
12 M_A_DQ34
12 M_A_DQ35
12 M_A_DQ36
12 M_A_DQ37
12 M_A_DQ38
12 M_A_DQ39
12 M_A_DQ40
12 M_A_DQ41
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12 M_A_DQ46
12 M_A_DQ47
12 M_A_DQ48
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12 M_A_DQ62
12 M_A_DQ63

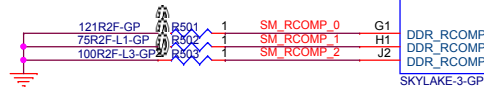
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12 M_A_CLK#0
12 M_A_CLK1
12 M_A_CLK#1
12 M_A_CLK2
12 M_A_CLK#2
12 M_A_CLK3
12 M_A_CLK#3
12 M_A_CS#0
12 M_A_CS#1
12 M_A_ODT0
12 M_A_ODT1
12 M_A_BA0
12 M_A_BA1
12 M_A_BG0
12 M_A_A16
12 M_A_A14
12 M_A_A15
12 M_A_A0
12 M_A_A1
12 M_A_A2
12 M_A_A3
12 M_A_A4
12 M_A_A5
12 M_A_A6
12 M_A_A7
12 M_A_A8
12 M_A_A9
12 M_A_A10
12 M_A_A11
12 M_A_A12
12 M_A_A13
12 M_A_BG1
12 M_A_ACT_N
12 M_A_PARITY
12 M_A_ALERT_N
12 M_A_DQS_DN0
12 M_A_DQS_DN1
12 M_A_DQS_DN2
12 M_A_DQS_DN3
12 M_A_DQS_DP4
12 M_A_DQS_DP5
12 M_A_DQS_DP6
12 M_A_DQS_DP7
12 M_A_DQS_DP0
12 M_A_DQS_DP1
12 M_A_DQS_DP2
12 M_A_DQS_DP3
12 M_A_DQS_DN4
12 M_A_DQS_DN5
12 M_A_DQS_DN6
12 M_A_DQS_DN7



SSID = CPU

13 M_B_DQ00	13 M_B_CLK0
13 M_B_DQ01	13 M_B_CLK#0
13 M_B_DQ02	13 M_B_CLK1
13 M_B_DQ03	13 M_B_CLK#1
13 M_B_DQ04	13 M_B_CLK#0
13 M_B_DQ05	13 M_B_CLK#1
13 M_B_DQ06	13 M_B_CLK#0
13 M_B_DQ07	13 M_B_CLK#1
13 M_B_DQ08	13 M_B_CLK#0
13 M_B_DQ09	13 M_B_CLK#1
13 M_B_DQ10	13 M_B_CLK#0
13 M_B_DQ11	13 M_B_CLK#1
13 M_B_DQ12	13 M_B_CLK#0
13 M_B_DQ13	13 M_B_CLK#1
13 M_B_DQ14	13 M_B_CLK#0
13 M_B_DQ15	13 M_B_CLK#1
13 M_B_DQ16	13 M_B_CLK#0
13 M_B_DQ17	13 M_B_CLK#1
13 M_B_DQ18	13 M_B_CLK#0
13 M_B_DQ19	13 M_B_CLK#1
13 M_B_DQ20	13 M_B_CLK#0
13 M_B_DQ21	13 M_B_CLK#1
13 M_B_DQ22	13 M_B_CLK#0
13 M_B_DQ23	13 M_B_CLK#1
13 M_B_DQ24	13 M_B_CLK#0
13 M_B_DQ25	13 M_B_CLK#1
13 M_B_DQ26	13 M_B_CLK#0
13 M_B_DQ27	13 M_B_CLK#1
13 M_B_DQ28	13 M_B_CLK#0
13 M_B_DQ29	13 M_B_CLK#1
13 M_B_DQ30	13 M_B_CLK#0
13 M_B_DQ31	13 M_B_CLK#1
13 M_B_DQ32	13 M_B_CLK#0
13 M_B_DQ33	13 M_B_CLK#1
13 M_B_DQ34	13 M_B_CLK#0
13 M_B_DQ35	13 M_B_CLK#1
13 M_B_DQ36	13 M_B_CLK#0
13 M_B_DQ37	13 M_B_CLK#1
13 M_B_DQ38	13 M_B_CLK#0
13 M_B_DQ39	13 M_B_CLK#1
13 M_B_DQ40	13 M_B_CLK#0
13 M_B_DQ41	13 M_B_CLK#1
13 M_B_DQ42	13 M_B_CLK#0
13 M_B_DQ43	13 M_B_CLK#1
13 M_B_DQ44	13 M_B_CLK#0
13 M_B_DQ45	13 M_B_CLK#1
13 M_B_DQ46	13 M_B_CLK#0
13 M_B_DQ47	13 M_B_CLK#1
13 M_B_DQ48	13 M_B_CLK#0
13 M_B_DQ49	13 M_B_CLK#1
13 M_B_DQ50	13 M_B_CLK#0
13 M_B_DQ51	13 M_B_CLK#1
13 M_B_DQ52	13 M_B_CLK#0
13 M_B_DQ53	13 M_B_CLK#1
13 M_B_DQ54	13 M_B_CLK#0
13 M_B_DQ55	13 M_B_CLK#1
13 M_B_DQ56	13 M_B_CLK#0
13 M_B_DQ57	13 M_B_CLK#1
13 M_B_DQ58	13 M_B_CLK#0
13 M_B_DQ59	13 M_B_CLK#1
13 M_B_DQ60	13 M_B_CLK#0
13 M_B_DQ61	13 M_B_CLK#1
13 M_B_DQ62	13 M_B_CLK#0
13 M_B_DQ63	13 M_B_CLK#1

12 V_SM_VREF_CNTA	13 V_SM_VREF_CNTB
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CPU1B SKYLAKE_HALO 2 OF 14

M_B_DQ00 BT11	DDR1_DQ0/DDR0_DQ16	DDR1_CKP0 AM9 M_B_CLK0
M_B_DQ01 BR11	DDR1_DQ1/DDR0_DQ17	DDR1_CKN0 AN9 M_B_CLK#0
M_B_DQ02 BT8	DDR1_DQ2/DDR0_DQ18	DDR1_CKP1 AM7 M_B_CLK1
M_B_DQ03 BR8	DDR1_DQ3/DDR0_DQ19	DDR1_CKN1 AN7 M_B_CLK#1
M_B_DQ04 BP11	DDR1_DQ4/DDR0_DQ20	DDR1_CKP2 AM10
M_B_DQ05 BN11	DDR1_DQ5/DDR0_DQ21	DDR1_CKN2 AJ10
M_B_DQ06 BP8	DDR1_DQ6/DDR0_DQ22	DDR1_CKP3 AJ11
M_B_DQ07 BN8	DDR1_DQ7/DDR0_DQ23	DDR1_CKN3 AJ12
M_B_DQ08 BL12	DDR1_DQ8/DDR0_DQ24	DDR1_CKE0 AT8 M_B_CKE0
M_B_DQ09 BL11	DDR1_DQ9/DDR0_DQ25	DDR1_CKE1 AT10 M_B_CKE1
M_B_DQ10 BL8	DDR1_DQ10/DDR0_DQ26	DDR1_CKE2 AT11
M_B_DQ11 BJ8	DDR1_DQ11/DDR0_DQ27	DDR1_CKE3 AT12
M_B_DQ12 BJ11	DDR1_DQ12/DDR0_DQ28	DDR1_CS0# AF11 M_B_CS#0
M_B_DQ13 BJ10	DDR1_DQ13/DDR0_DQ29	DDR1_CS1# AE7 M_B_CS#1
M_B_DQ14 BL7	DDR1_DQ14/DDR0_DQ30	DDR1_CS2# AF10
M_B_DQ15 BJ7	DDR1_DQ15/DDR0_DQ31	DDR1_CS3# AE10
M_B_DQ16 BG11	DDR1_DQ16/DDR0_DQ48	DDR1_ODT0 AF7 M_B_ODT0
M_B_DQ17 BG10	DDR1_DQ17/DDR0_DQ49	DDR1_ODT1 AE8 M_B_ODT1
M_B_DQ18 BG8	DDR1_DQ18/DDR0_DQ50	DDR1_ODT2 AE9
M_B_DQ19 BF8	DDR1_DQ19/DDR0_DQ51	DDR1_ODT3 AE11
M_B_DQ20 BF11	DDR1_DQ20/DDR0_DQ52	DDR1_RAS#/DDR1_CAB3/DDR1_MA16
M_B_DQ21 BF10	DDR1_DQ21/DDR0_DQ53	DDR1_WE#/DDR1_CAB2/DDR1_MA14
M_B_DQ22 BG7	DDR1_DQ22/DDR0_DQ54	DDR1_CAS#/DDR1_CAB1/DDR1_MA15
M_B_DQ23 BF7	DDR1_DQ23/DDR0_DQ55	DDR1_BA0/DDR1_CAB4/DDR1_BA0
M_B_DQ24 BB11	DDR1_DQ24/DDR0_DQ56	DDR1_BA1/DDR1_CAB6/DDR1_BA1
M_B_DQ25 BC11	DDR1_DQ25/DDR0_DQ57	DDR1_BA2/DDR1_CAA5/DDR1_BA0
M_B_DQ26 BB8	DDR1_DQ26/DDR0_DQ58	DDR1_MA0/DDR1_CAB9/DDR1_MA0
M_B_DQ27 BC8	DDR1_DQ27/DDR0_DQ59	DDR1_MA1/DDR1_CAB8/DDR1_MA1
M_B_DQ28 BC10	DDR1_DQ28/DDR0_DQ60	DDR1_MA2/DDR1_CAB5/DDR1_MA2
M_B_DQ29 BB10	DDR1_DQ29/DDR0_DQ61	DDR1_MA3
M_B_DQ30 BC7	DDR1_DQ30/DDR0_DQ62	DDR1_MA4
M_B_DQ31 BB7	DDR1_DQ31/DDR0_DQ63	DDR1_MA5/DDR1_CAA0/DDR1_MA5
M_B_DQ32 AA11	DDR1_DQ32/DDR1_DQ16	DDR1_MA6/DDR1_CAA2/DDR1_MA6
M_B_DQ33 AA10	DDR1_DQ33/DDR1_DQ17	DDR1_MA7/DDR1_CAA4/DDR1_MA7
M_B_DQ34 AC11	DDR1_DQ34/DDR1_DQ18	DDR1_MA8/DDR1_CAA3/DDR1_MA8
M_B_DQ35 AC10	DDR1_DQ35/DDR1_DQ19	DDR1_MA9/DDR1_CAA1/DDR1_MA9
M_B_DQ36 AA7	DDR1_DQ36/DDR1_DQ20	DDR1_MA10/DDR1_CAB7/DDR1_MA10
M_B_DQ37 AA8	DDR1_DQ37/DDR1_DQ21	DDR1_MA11/DDR1_CAA7/DDR1_MA11
M_B_DQ38 AC8	DDR1_DQ38/DDR1_DQ22	DDR1_MA12/DDR1_CAA6/DDR1_MA12
M_B_DQ39 AC7	DDR1_DQ39/DDR1_DQ23	DDR1_MA13/DDR1_CAB0/DDR1_MA13
M_B_DQ40 W8	DDR1_DQ40/DDR1_DQ24	DDR1_MA14/DDR1_CAA9/DDR1_MA14
M_B_DQ41 W7	DDR1_DQ41/DDR1_DQ25	DDR1_MA15/DDR1_CAA8/DDR1_MA15
M_B_DQ42 V10	DDR1_DQ42/DDR1_DQ26	DDR1_PAR AJ7 M_B_PARITY
M_B_DQ43 V11	DDR1_DQ43/DDR1_DQ27	DDR1_ALERT# AR8 M_B_ALERT_N
M_B_DQ44 W11	DDR1_DQ44/DDR1_DQ28	
M_B_DQ45 W10	DDR1_DQ45/DDR1_DQ29	
M_B_DQ46 V7	DDR1_DQ46/DDR1_DQ30	
M_B_DQ47 V8	DDR1_DQ47/DDR1_DQ31	
M_B_DQ48 R11	DDR1_DQ48	
M_B_DQ49 P11	DDR1_DQ49	
M_B_DQ50 P7	DDR1_DQ50	
M_B_DQ51 R8	DDR1_DQ51	
M_B_DQ52 R10	DDR1_DQ52	
M_B_DQ53 P8	DDR1_DQ53	
M_B_DQ54 R7	DDR1_DQ54	
M_B_DQ55 L11	DDR1_DQ55	
M_B_DQ56 M11	DDR1_DQ56	
M_B_DQ57 L7	DDR1_DQ57	
M_B_DQ58 M8	DDR1_DQ58	
M_B_DQ59 L10	DDR1_DQ59	
M_B_DQ60 M10	DDR1_DQ60	
M_B_DQ61 M7	DDR1_DQ61	
M_B_DQ62 L8	DDR1_DQ62	
M_B_DQ63 L8	DDR1_DQ63	
AW11	DDR1_ECC0	
AY11	DDR1_ECC1	
AY8	DDR1_ECC2	
AY10	DDR1_ECC3	
AW10	DDR1_ECC4	
AY7	DDR1_ECC5	
AY9	DDR1_ECC6	
AW7	DDR1_ECC7	

DDR CHANNEL B

SKYLAKE-3-GP

AROUND_CPU

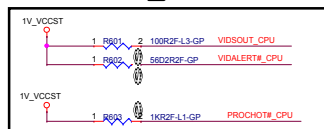


Figure 43-1. KBL H Flow Diagram for SYS_PWROK/PCU_PWROK Generation

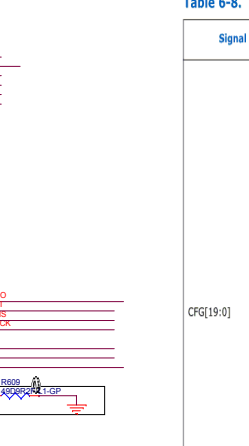
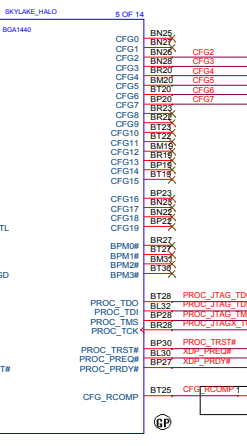
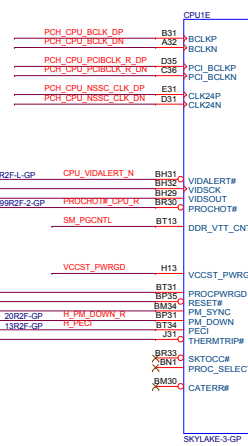
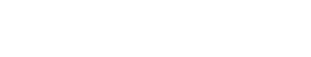
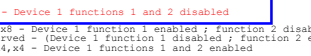
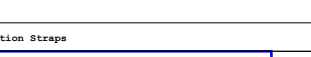
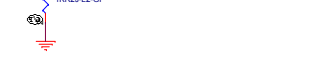
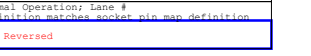
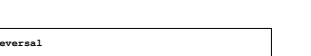
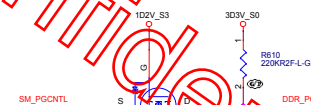
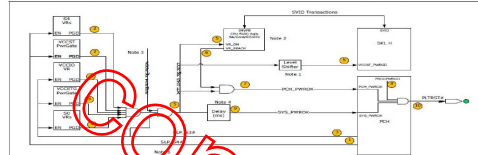


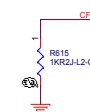
Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: <ul style="list-style-type: none"> 1 = (Default) Normal Operation; No stall. 0 = Stall. CFG[1]: Reserved configuration lane. CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> 1 = Normal operation 0 = Lane numbers reversed. CFG[3]: Reserved configuration lane. CFG[4]: eDP enable: <ul style="list-style-type: none"> 1 = Disabled. 0 = Enable. CFG[6:5]: PCI Express* Bifurcation <ul style="list-style-type: none"> 00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express* CFG[7]: PEG Training: <ul style="list-style-type: none"> 1 = (default) PEG Train immediately following RESET# de assertion 0 = PEG Wait for BIOS for training. CFG[19:8]: Reserved configuration lanes. 	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

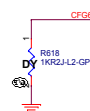
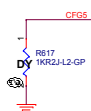
PEG Static Lane Reversal
CFG2
1: Normal Operation; Lane # definition matches socket pin map definition
0: Lane Reversed



eDP Enable
CFG4
1: Disable
0: Enable



PCIe Port Bifurcation Straps
CFG[6:5]
11: x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



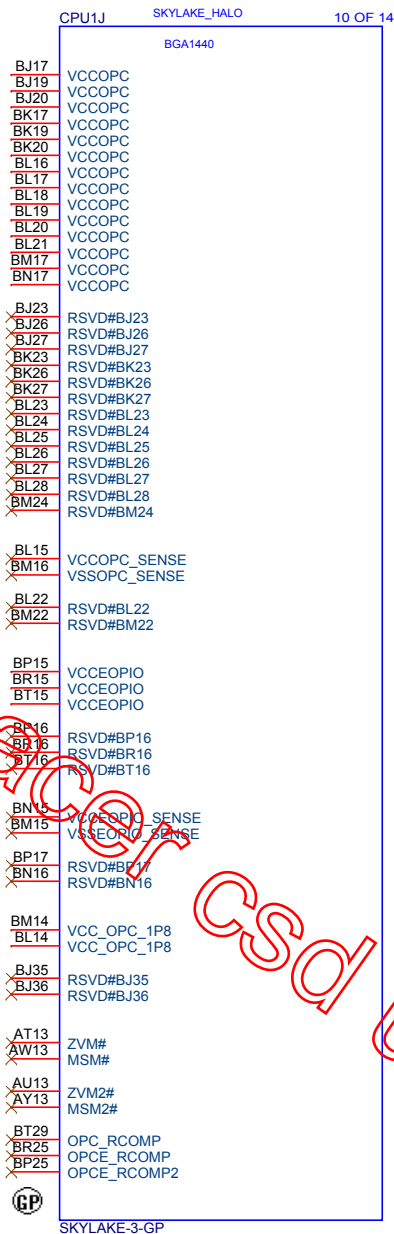
Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	VCC _{IO}	16-60 Ω
PREQ#	Pull Up	VCC _{ST}	3 kΩ
PROC_TDI	Pull Up	VCC _{STG} ¹	3 kΩ
PROC_TMS	Pull Up	VCC _{SGT} ¹	3 kΩ
PROC_TRST#	Pull Down	-	3 kΩ
CFG[19:0]	Pull Up	VCC _{IO}	3 kΩ

Notes:
1. For S-Processor line, it should be VCC_{ST}

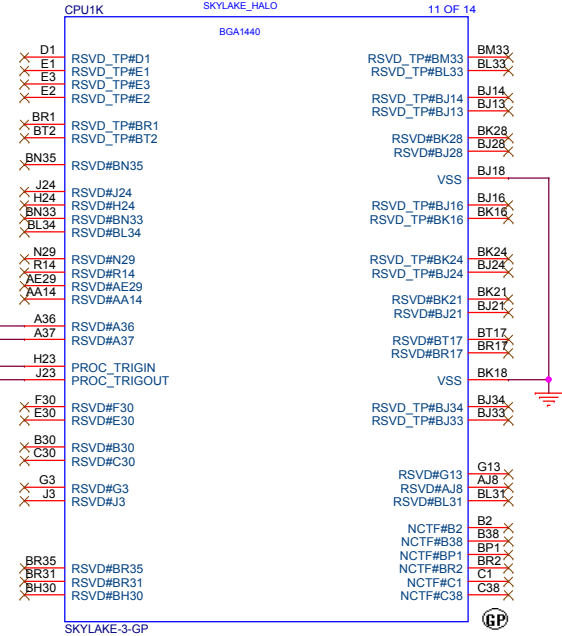
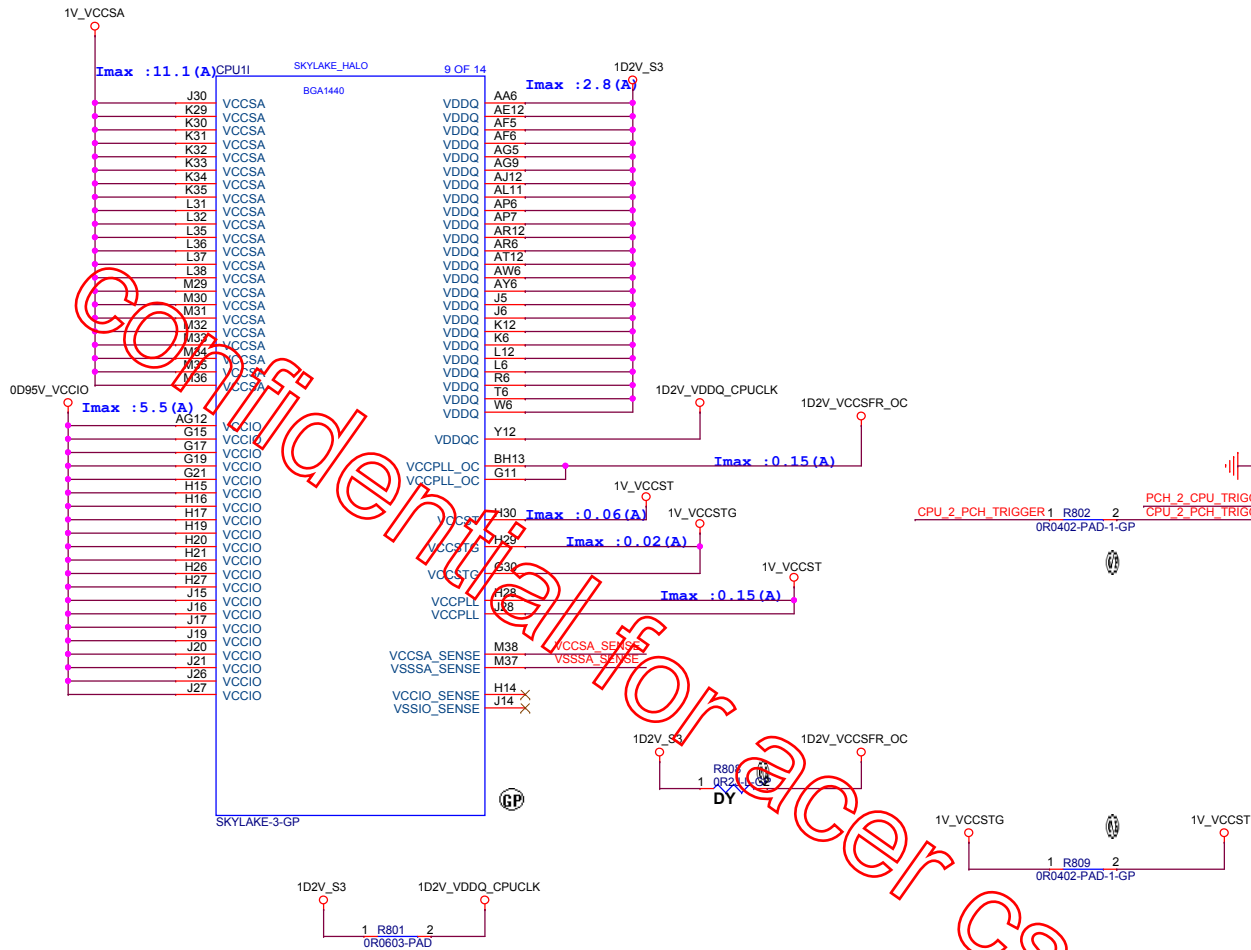
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File	CPU_CFG_CFG_STRAP
Size	Document Number
Date	Version
Neptune KLS Date: 2017/05/17 Rev: 1.0	



Title: CPU_POWER1 (ASIC Power Bolck)			
Size Customr	Document Number: Neptune_KLS	Rev	-1m
Date: Wednesday, May 11, 2017	Sheet 7	of	105

23 PCH_2_CPU_TRIGGER >>>=
23 CPU_2_PCH_TRIGGER <<<=
46 VCCSA_SENSE <<<=
46 VSSSA_SENSE <<<=





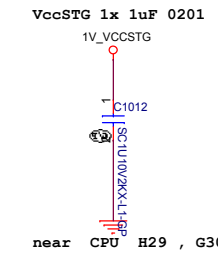
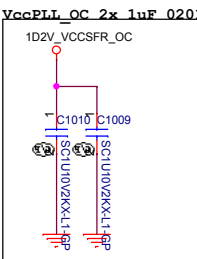
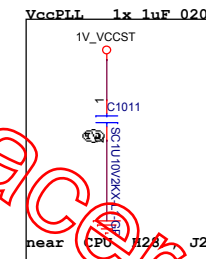
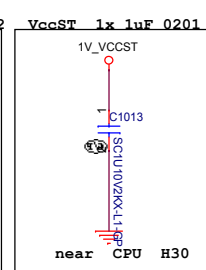
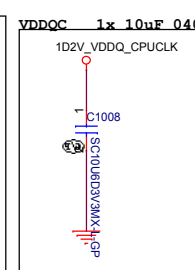
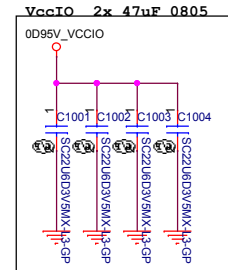
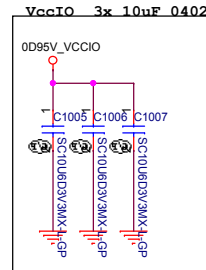
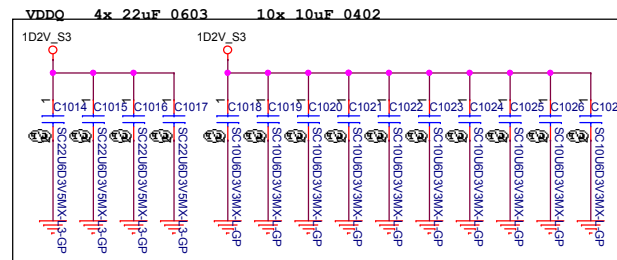
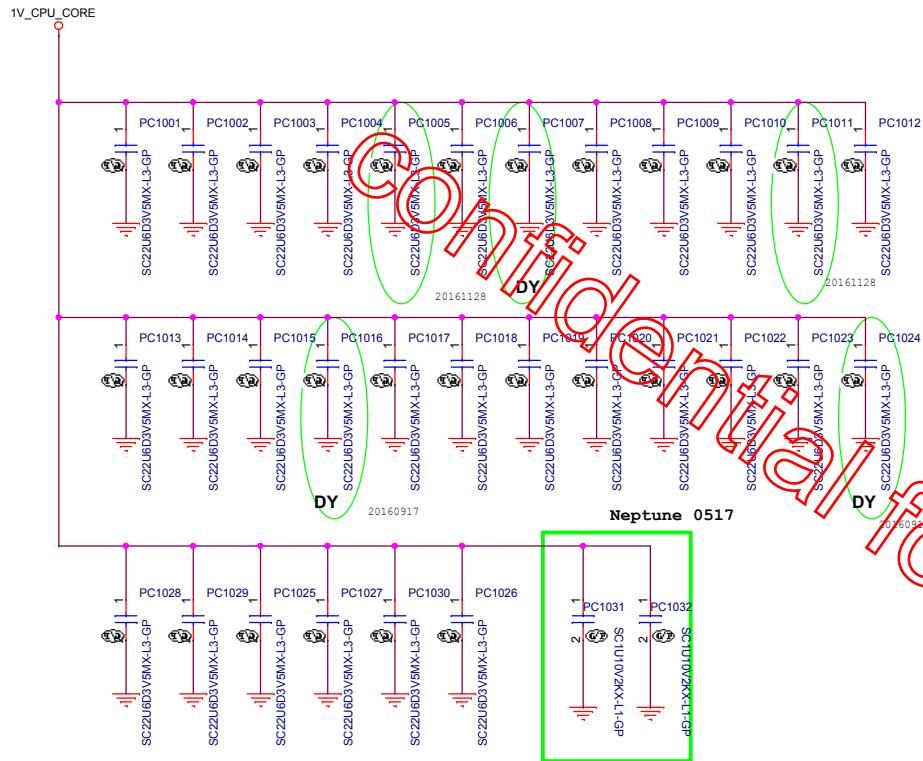


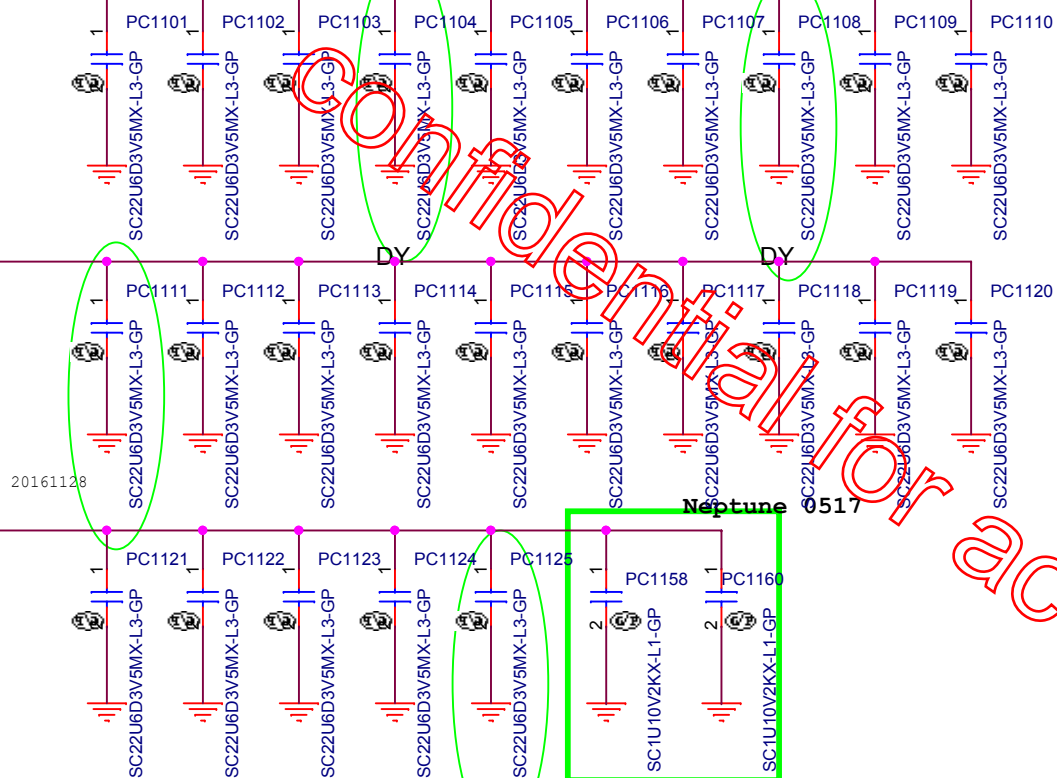
Table 49-3. Decoupling Requirements for KBL H Processor

Domain	Board Edge cap	Package cap	Notes
Vcc	4x 47uF 0805	8x 22uF 0603 8x 22uF 0805 28x 10uF 0402 63x 1uF 0201	
VccGT	6x 47uF 0805	8x 22uF 0603 35x 10uF 0402 68x 1uF 0201	
VccGTx	8x 22uF 0603	4x 10uF 0402 12x 1uF 0201	Only needed when supporting 44e Only needed when supporting 44e
VccGA	1x 47uF 0805	1x 47uF 0805 7x 10uF 0402 3x 1uF 0201	
VDDQ		4x 22uF 0603 10x 10uF 0402	
VDDQC		1x 10uF 0402	
VccIO		3x 10uF 0402	
VccST		1x 1uF 0201	Do not route VccST closest adjacent layer over any power net other than ground.
VccSTG		1x 1uF 0201	Share supply with 1.0V PCH rail
VccPLL		1x 1uF 0201	Do not route VccPLL, VccSTG closest adjacent layer over any power net other than ground.
VccPLL_OC		2x 1uF 0201	Share with VDDQ. Do not route VccPLL_OC closest adjacent layer over any power net other than ground.
VccOPC		10x 10uF 0402	Only needed when supporting 44e VR: +/-5% or +/-50mV
VccQPRIO		3x 10uF 0402	Only needed when supporting 44e VR: +/-5% or +/-50mV

<Core Design>

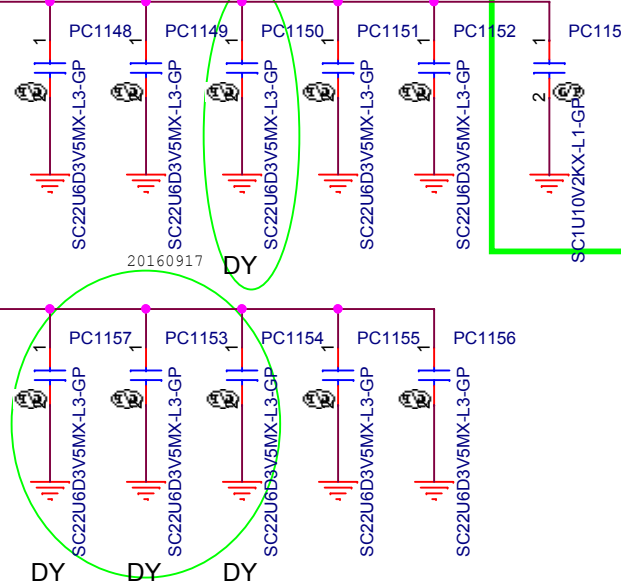
1V_VCCGT

20160917



1V_VCCSA

Neptune 0517



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Title

CPU (Power CAP2)

Size
A4

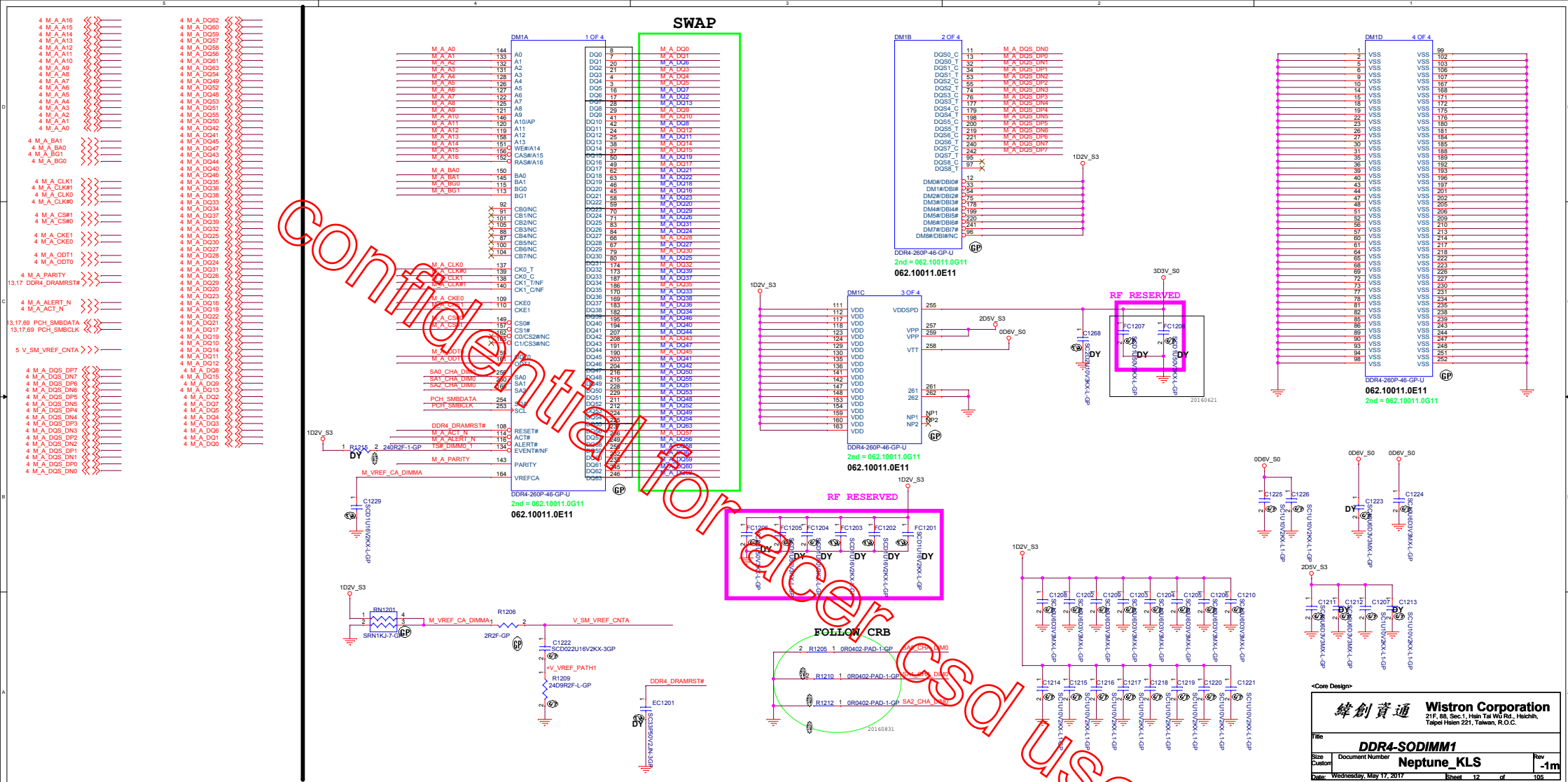
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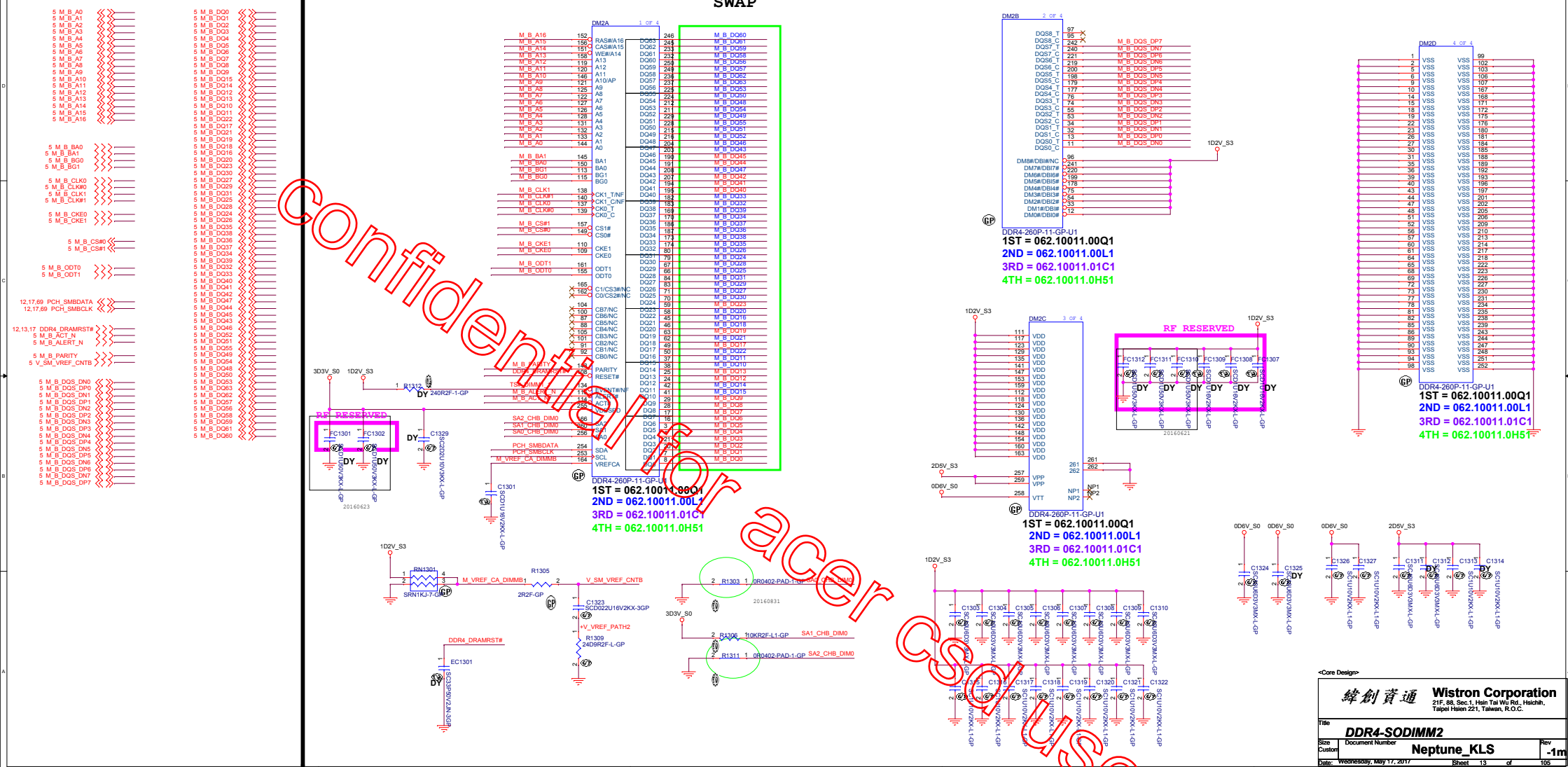
Neptune_KLS

Rev
-1m

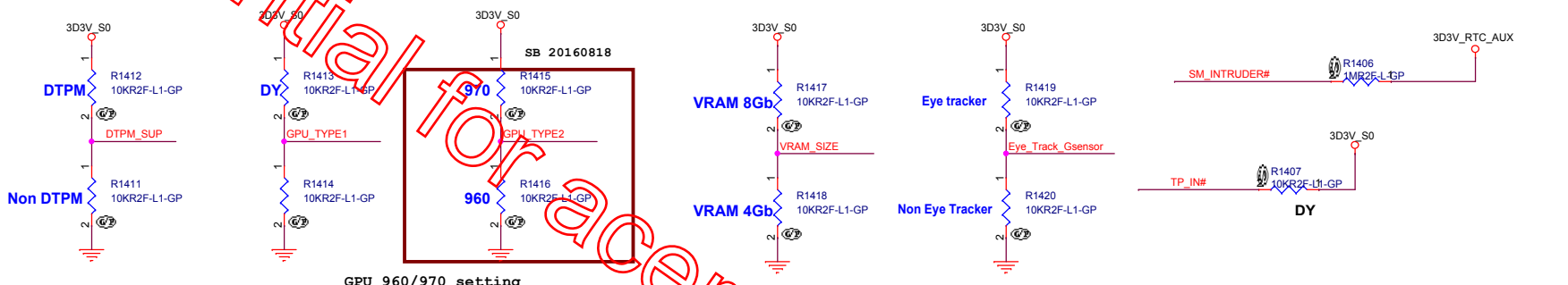
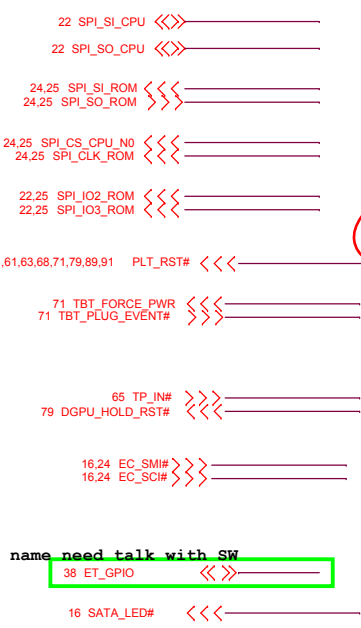
Date: Wednesday, May 17, 2017

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00:960 10:970 01: Reserve 11: Reserve (Type2:Type1)

	GPU_TYPE2	
	0	1
GPU_TYPE1	0	960
	1	970
	0	Reserve
	1	Reserve

	DTPM_SUP	Eye_Track_Gsensor	VRAM_SIZE
0	NO	NO	VRAM 4Gb
1	YES	YES	VRAM 8Gb

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SSID = PCH

```
71 TBT_PCIE_WAKE#_PCH >>>_____
```

14,24 EC_SCI# <<< _____

MSATA

63 SLOT1X4_PCIE_TX_P2 <<< _____
63 SLOT1X4_PCIE_TX_N2 <<< _____
63 SLOT1X4_PCIE_RX_P2 <<< _____
63 SLOT1X4_PCIE_RX_N2 <<< _____

MSATA

63 SLOT1X4_PCIE_TX_P3 <<< _____
63 SLOT1X4_PCIE_TX_N3 <<< _____
63 SLOT1X4_PCIE_RX_P3 <<< _____
63 SLOT1X4_PCIE_RX_N3 <<< _____

MSATA

```
63 SLOT1X4_PCIE_RX_N0 >>> _____
63 SLOT1X4_PCIE_RX_P0 >>> _____
63 SLOT1X4_PCIE_TX_N0 <<< _____
63 SLOT1X4_PCIE_TX_P0 <<< _____
```

```

63 SLOT1X4_PCIE_RX_N1  >>>
63 SLOT1X4_PCIE_RX_P1  >>>
63 SLOT1X4_PCIE_TX_N1  >>>
63 SLOT1X4_PCIE_TX_P1  >>>

```

63 SATAGP0 <<<_____

HDD 1

```

60 HDD1_SATA_RX_N  >>>>>
60 HDD1_SATA_RX_P  >>>>>
60 HDD1_SATA_TX_N  <<<<<
60 HDD1_SATA_TX_P  <<<<<

```

eDP

```
55 eDP_BLCTRL_CPU  <<< _____
24 eDP_BLEN_CPU    <<< _____
55 eDP_VDDEN_CPU   <<< _____
```

```

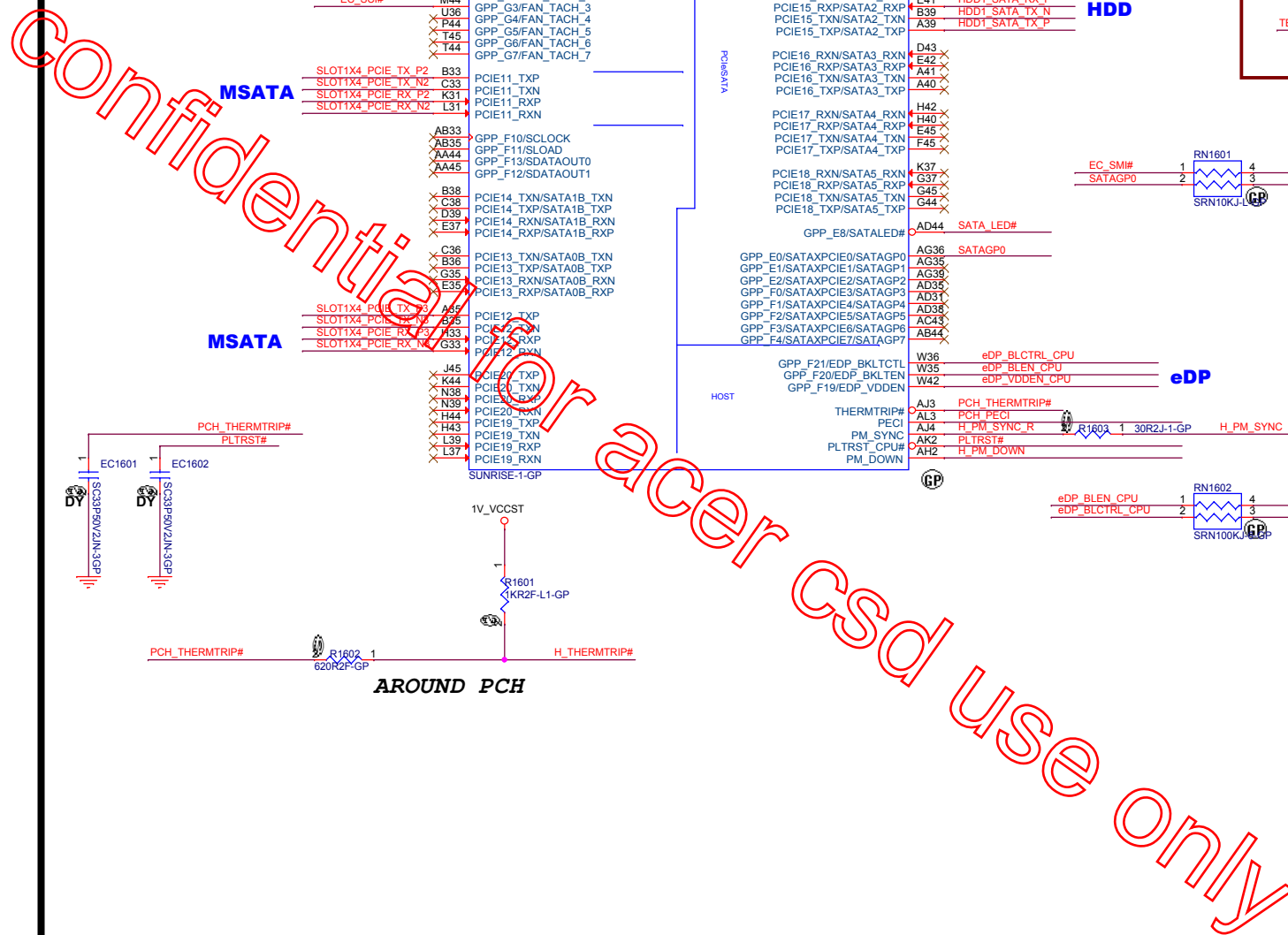
6 PCH_PECI    >>> _____
6 H_PM_SYNC   >>> _____
6 PLTRST#     >>> _____
6 H_PM_DOWN   >>> _____

```

6 H_THERMTRIP# >>>_____

14,24 EC_SMI# <<<_____

14 SATA_LED# >>>_____

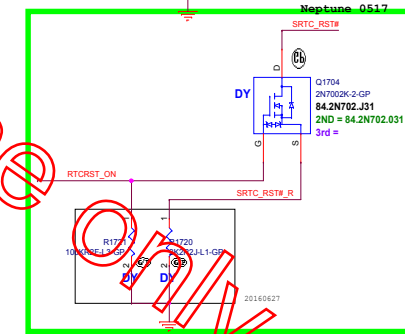
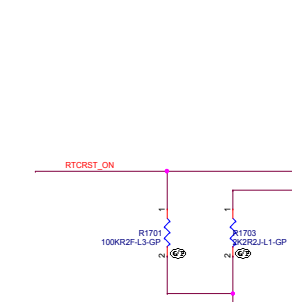
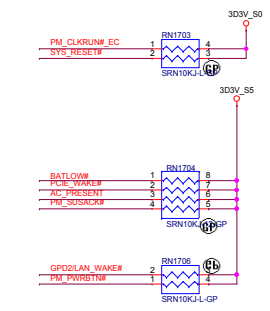
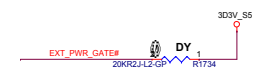
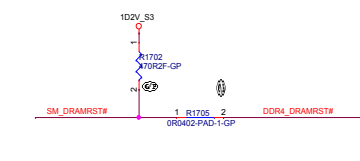
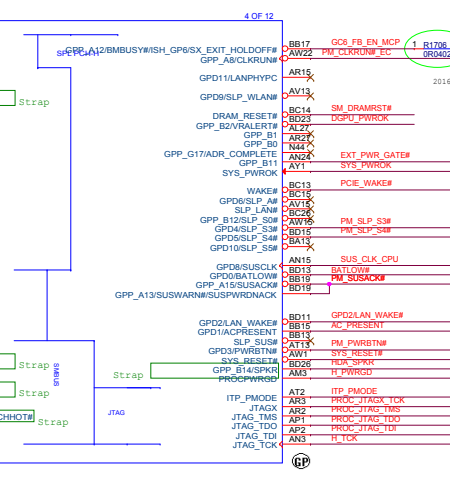
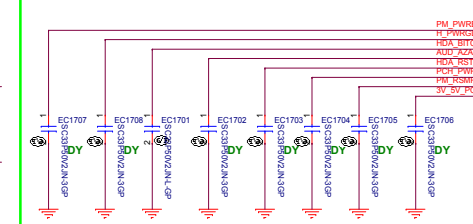
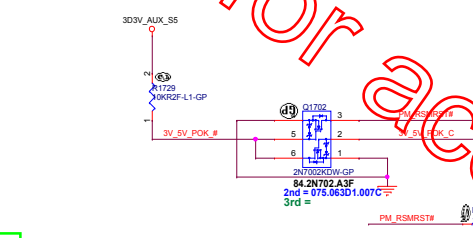
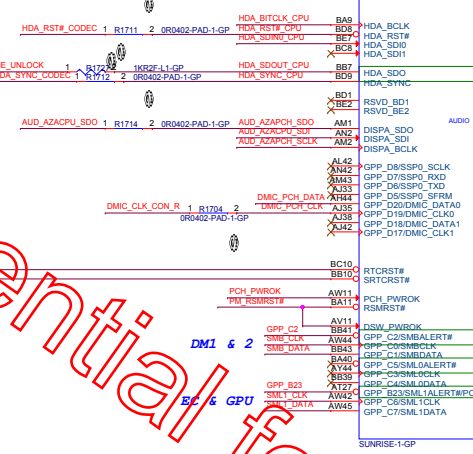
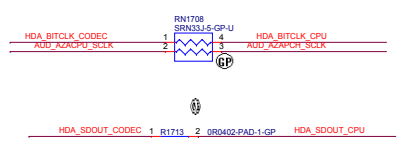
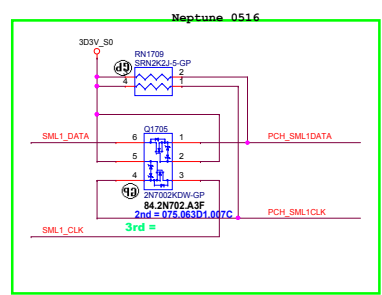
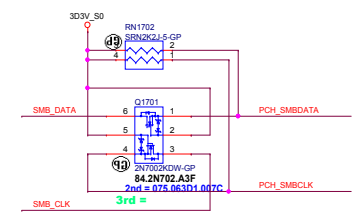
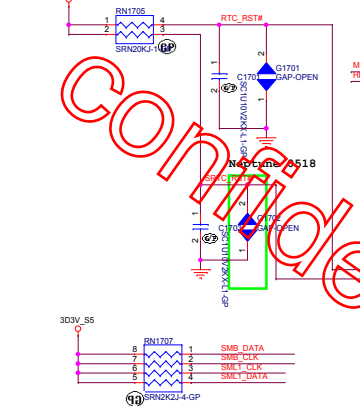
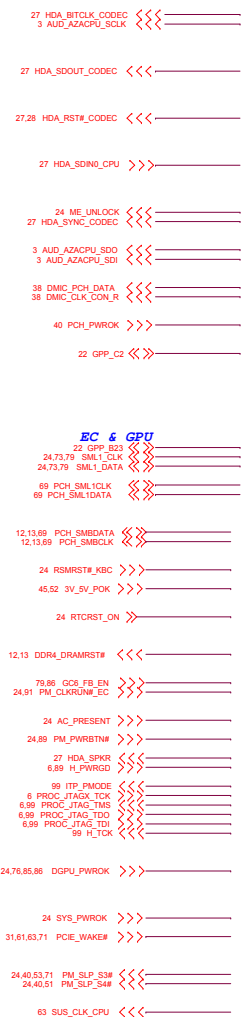


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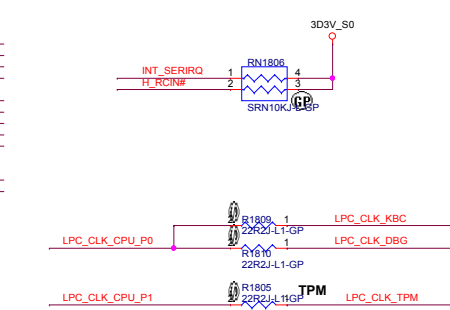
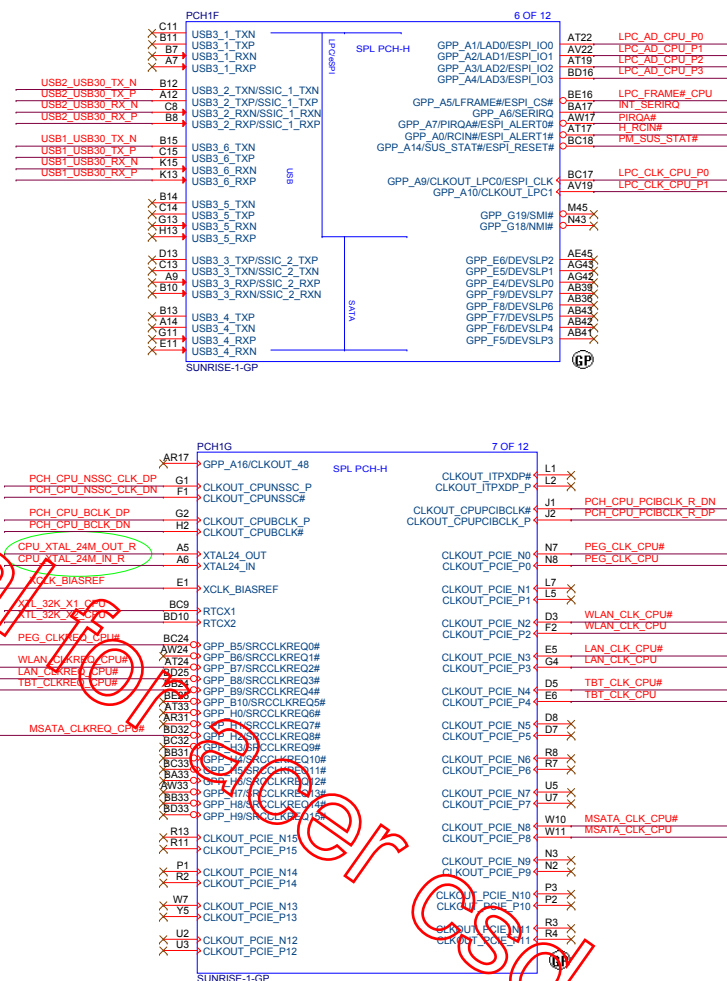
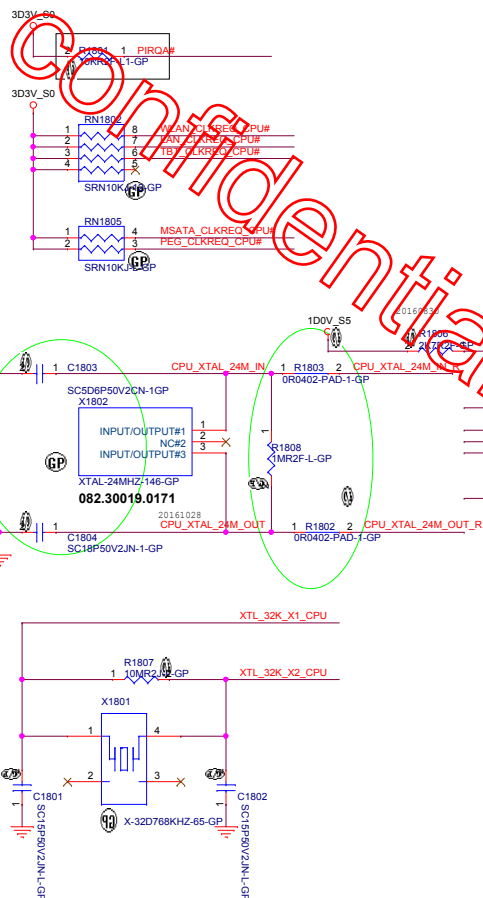
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Title			
PCH_PCIE_SATA			
Size A3	Document Number		Rev
	Neptune_KLS		-1m
Date:	Wednesday, May 17, 2017	Sheet 16 of	105

SSID = PCH



SSID = PCH



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Title				PCH USB3 CLOCK			
Size	Document Number			Rev			
Custom	Neptune_KLS			-1			
Date	Wednesday, May 17, 2017			Sheet	18	of	105

```
18,71 TBT_CLK_CPU# <<< _____
18,71 TBT_CLK_CPU <<< _____
```

```
71 DDI1_TBT_HPD_CPU >>> _____
71 DDI2_TBT_HPD_CPU >>> _____
```

```
55 eDP_HPD_CPU >>> _____
65 KB_BL_DET >>> _____
```

22 DDI2_TBT_DATA_CPU << >> _____
71 DDI1_TBT_CLK_CPU << >> _____
71 DDI1_TBT_DATA_CPU << >> _____

22 DDPD_DATA_CPU << >> _____

```

22 GPP_B22/GSPI1_MOSI <<>>=====
86 DGPU_PWR_EN# <<<>>=====

```

25 RTC_DET# <<<_____

22 GPP_B18/GSPI0_MOSI <<>> _____
79 GPU_EVENT# >>>> _____

61,89 BLUETOOTH_EN <<< _____
61 WIFI RF_EN <<< _____

TOUCH PAD

```

65 I2C1_CLK_CPU <=> _____
65 I2C1_DATA_CPU <=> _____

```

Neptune 0516

G-sensor

```

24 I2C2_CLK_CPU <<>>_____
24 I2C2_DATA_CPU <<>>_____
24,38,69 EYETRACKER_INT# <<>>_____

```

```

57 I2C0_CLK_CPU_TIMER  << >> _____
57 I2C0_DATA_CPU_TIMER  << >> _____

```

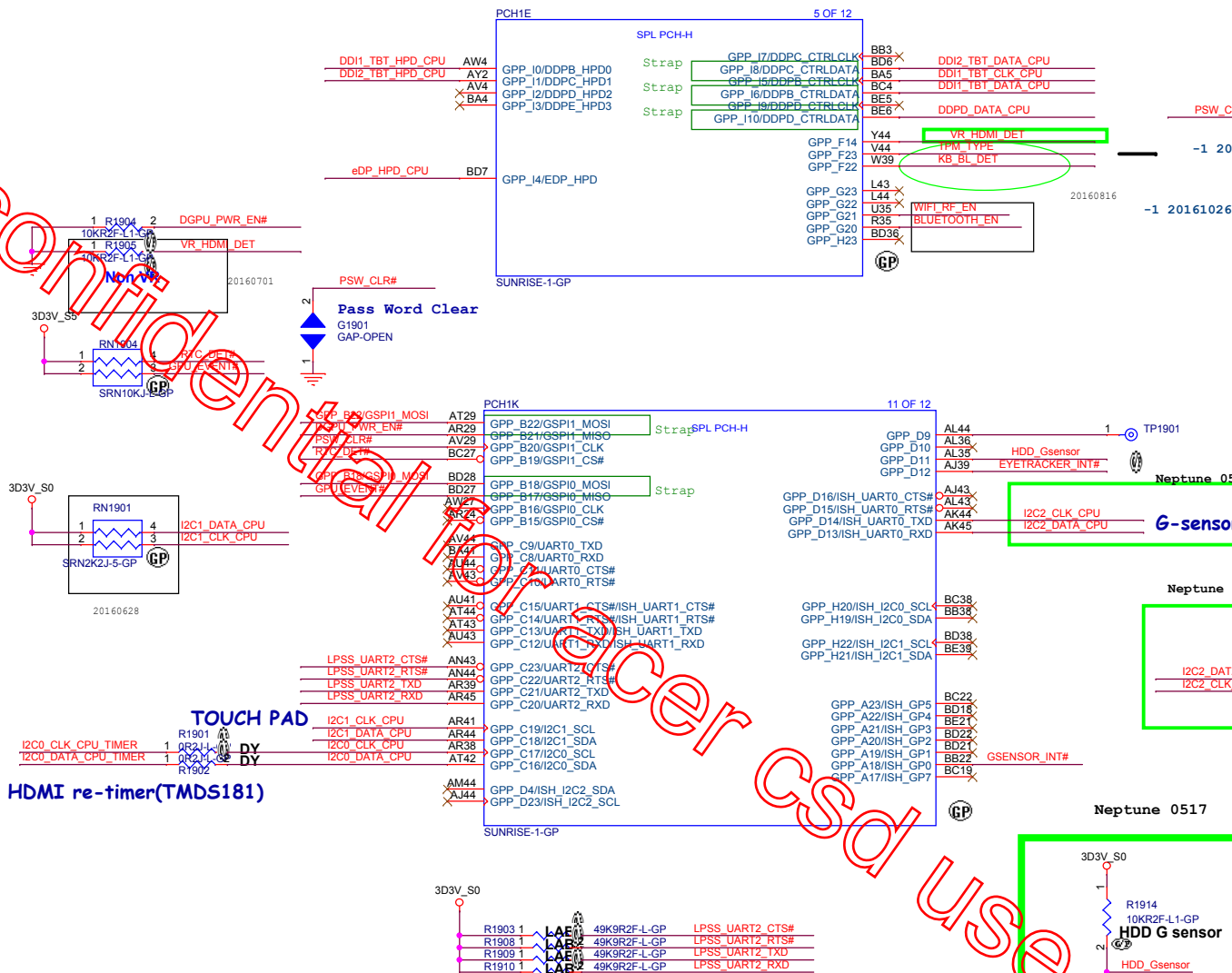
69 GSENSOR INT# <<<_____

68 LPSS_UART2_TXD <<< _____

68 LPSS_UART2_RXD <<< _____

57 VR HDMI DET >>>

check



Neptune 0517

10KR2F-L1-GP
HDD G sensor

Non HDD Sensor

```
1 Support
0 no support
```

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

PCH GPP2 GPP3

Size

Document Number

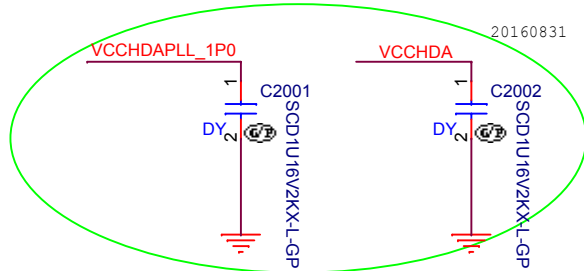
Neptune_KLS

Rev

-1m

Date: Wednesday, May 17, 2017

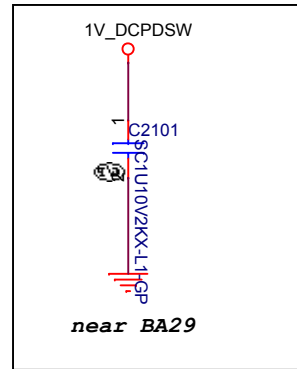
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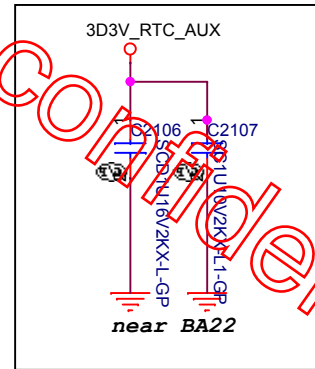
Date: Wednesday, May 17, 2017 Sheet 20 of 105

SSID = PCH

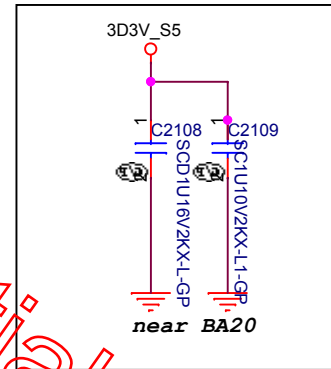
DcpDSW
1x 1uF



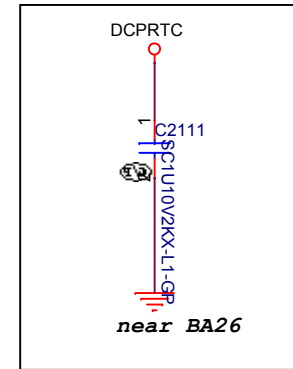
VccRTC
1x1 uF 1x0.1 uF



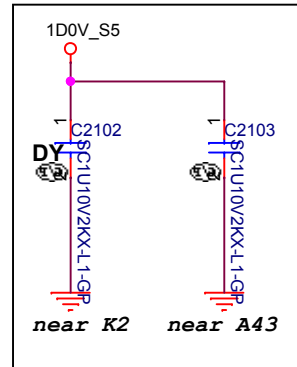
VccRTCPRIM
1x1 uF 1x0.1 uF



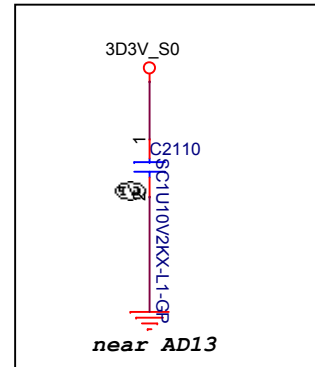
DcpRTC
1x 0.1uF



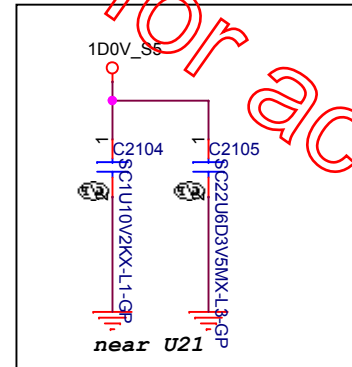
VccMPHYPLL / VccPCIE3PLL
1x1 uF



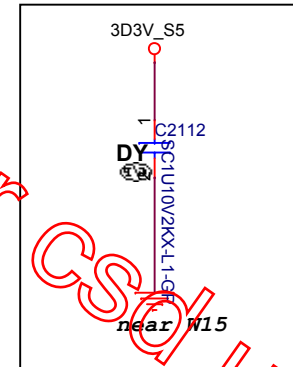
VccATS
1x1 uF



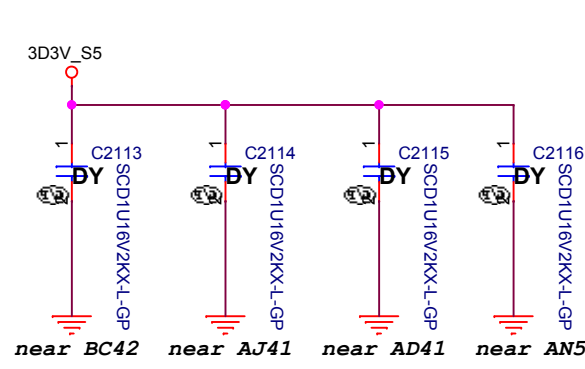
VccMPHY / VccPRIM / VccAPLLEBB
1x1 uF 1x22 uF



VccDSW
1x 1uF



VccPGPPBCH / VccPGPPEF / VccPGPPG
/ VccPRIM
4x 0.1 uF



Decoupling and Power Connection Requirements for SKL S/H PCH (DT / AIO)
(Sheet 1 of 2)

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R/jumper / E/edge)	Place capacitor(s) near ball(s)
V1.0A	VccMPHY VccPRIM VccAPLLEBB	U21, U23, U25, U26, V26, AC17, V28	1 uF 22 uF	0402 0805	1	E (<3 mm)	U21
	VccMPHYPLL VccPCIE3PLL	A43, B43, C44, C45	1 uF	0402	1	E (<5 mm)	A43
	VccCLK5	K2, K3	1 uF	0402	1	E (<5 mm)	K2 (Note 1)
	VccCLK (1,2,3,4,6)	N17, R19, U20, V17, R17	-	-	-	-	-
	VccUSB2PLL VccHDAPLL	AJ5, AL5, AN19	-	-	-	-	-
	VccPRIM	AL22	-	-	-	-	-
	VccPRIM	AD15	-	-	-	-	-
	VccPRIM	AJ20, AJ21, AJ23, AJ25	-	-	-	-	-
	VccPRIM	AA23, AA36, AA38, AC13, AC26, AC28, AE23, AE26, Y23, Y25	-	-	-	-	-
	VccPRIM	-	-	-	-	-	-
V1.0DS W	DcpDSW	BA29	1 uF	0402	1	E (<5 mm)	BA29
V1.8A/ V3.3A	VccPGPPBCH	BC42, BD40	0.1 uF	0402	1	E (<3 mm)	BC42 (Note 1)
	VccPGPPEF	AJ41, AL41	0.1 uF	0402	1	E (<3 mm)	AJ41 (Note 1)
	VccPGPPG	AD41	0.1 uF	0402	1	E (<3 mm)	AD41 (Note 1)
	VccPRIM	AN5	0.1 uF	0402	1	E (<3 mm)	AN5 (Note 1)
	VccPGPPA	BA31	-	-	-	-	-
	VccSPT	BE41, BE42, BE43	-	-	-	-	-
V1.8A/ V1.8S/ V3.3S	VccATS	AD13	1 uF	0402	1	E (<5 mm)	AD13
V1.5A/ V1.8A/ V3.3A	VccHDA	BA15	-	-	-	-	-
V3.3A	VccRTCPRIM	BA20	1 uF 0.1 uF	0402 0402	1 1	E (<5 mm) E (<3 mm)	BA20
	VccPRIM	BD3, BE3, BE4	-	-	-	-	-
V3.3RTC	VccRTC	BA22	1 uF 0.1 uF	0402 0402	1 1	E (<5 mm) E (<3 mm)	BA22
	VccDSW	W15	1 uF	0401	1	E (<3 mm)	W15 (Note 1)
V3.3DS W	VccDSW	BA24	-	-	-	-	-
PCH Internal VRM	DcpRTC	BA26	0.1 uF	0402	1	E (<5 mm)	BA26

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Title		PCH_POWER_CAP1	
Size A4	Document Number	Rev	
Neptune_KLS		-1m	
Date: Wednesday, May 17, 2017		Sheet 21 of 105	

Description	Display Port B Detected	Display Port C Detected	Display Port D Detected	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	ESPI FLASH SHARING MODE
GPIO	GPP_I6	GPP_I8	GPP_I10	GPP_B18	GPP_B22	HDA_SDO	GPP_H12
Schematic							
High	Detected	Detected	Detected	Enable	LPC	Disable	1: SLAVE ATTACHED FLASH SHARING ESPI FLASH SHARING MODE
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	0: MASTER ATTACHED FLASH SHARING
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	eSPI or LPC	TLS Confidentiality	Reserved	Reserved	Reserved	Reserved	Reserved
GPIO	GPP_B14	GPP_C5	GPP_C2	SPI0_IO3	SPI0_IO2	SPI0_MOSI	SPI0_MISO	GPP_B23 / PCHHOT#
Schematic								
High	Enable	eSPI	Enable					
Low	Disable	LPC	Disable					
	internal pull-down	internal pull-down	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-down

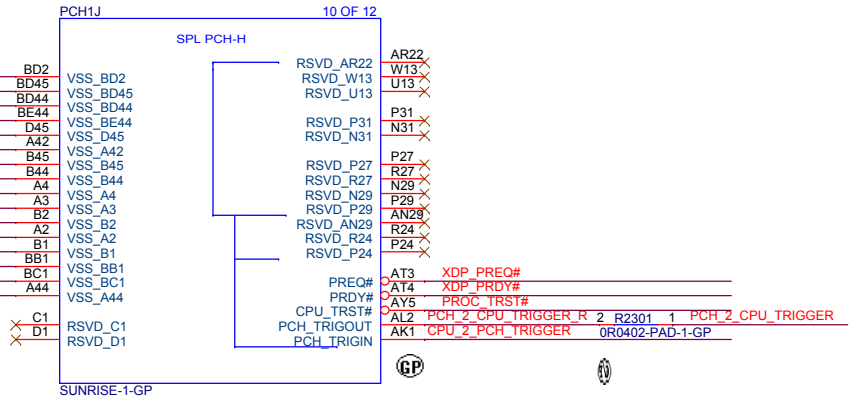
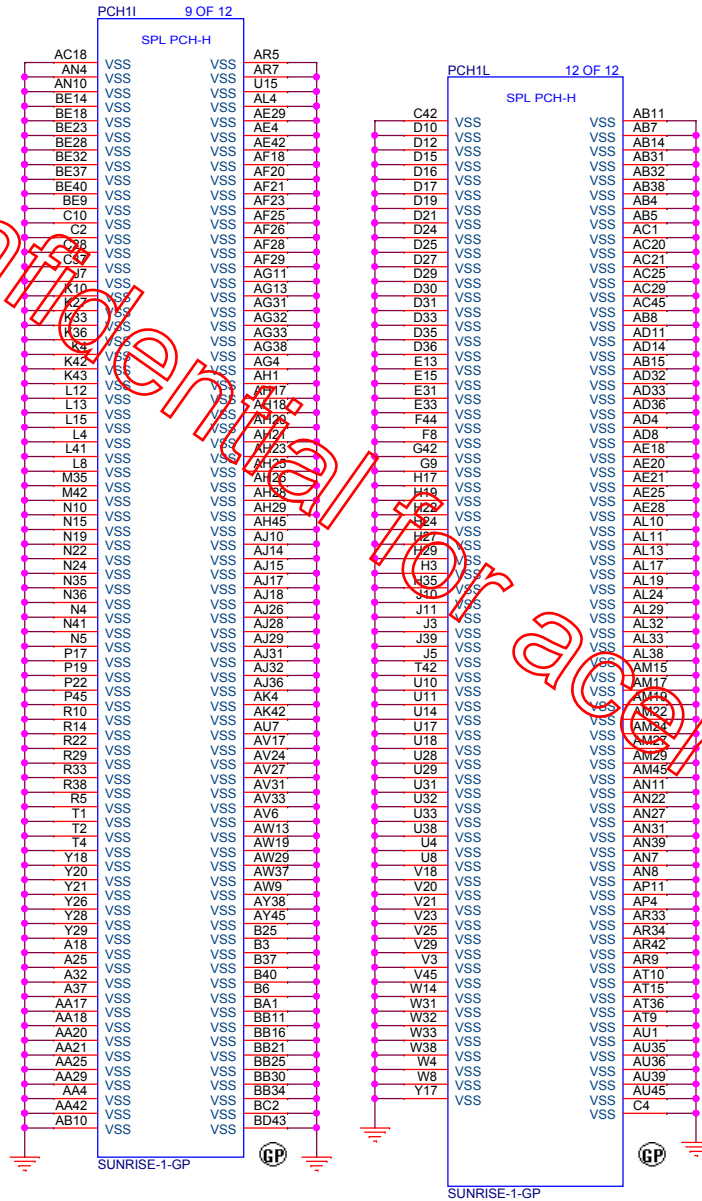
[H,S,U,Y] Pull-up Resistors on SPI_IO2 and SPI_IO3 Requirement Update

The current Skylake Platform Design Guide (PDG) states that a 1 K pull-up resistor is required on the PCH SPI_IO2 and SPI_IO3 signals.

This 1K pull up resistor is no longer needed on Skylake platform and can be removed from the motherboard. The new guidelines will be updated in a future release of the Skylake PDG.

SSID = PCH

6.99 XDP_PREQ# >>> _____
6.99 XDP_PRDY# >>> _____
6.99 PROC_TRST# >>> _____
8 PCH_2_CPU_TRIGGER >>> _____
8 CPU_2_PCH_TRIGGER >>> _____



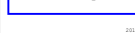
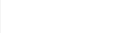
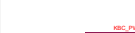
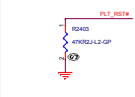
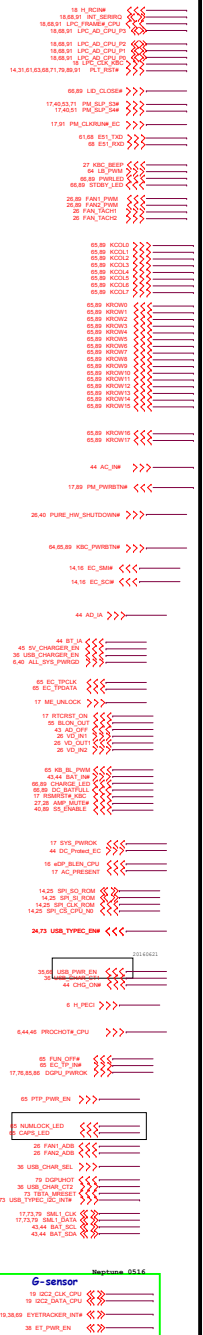
<Core Design>

緯創資通

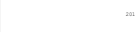
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			PCH_RSVD_VSS	
Size	Document Number	Neptune_KLS		Rev
B				-1m
Date:	Wednesday, May 17, 2017	Sheet	23	of 105

SSID = KBC

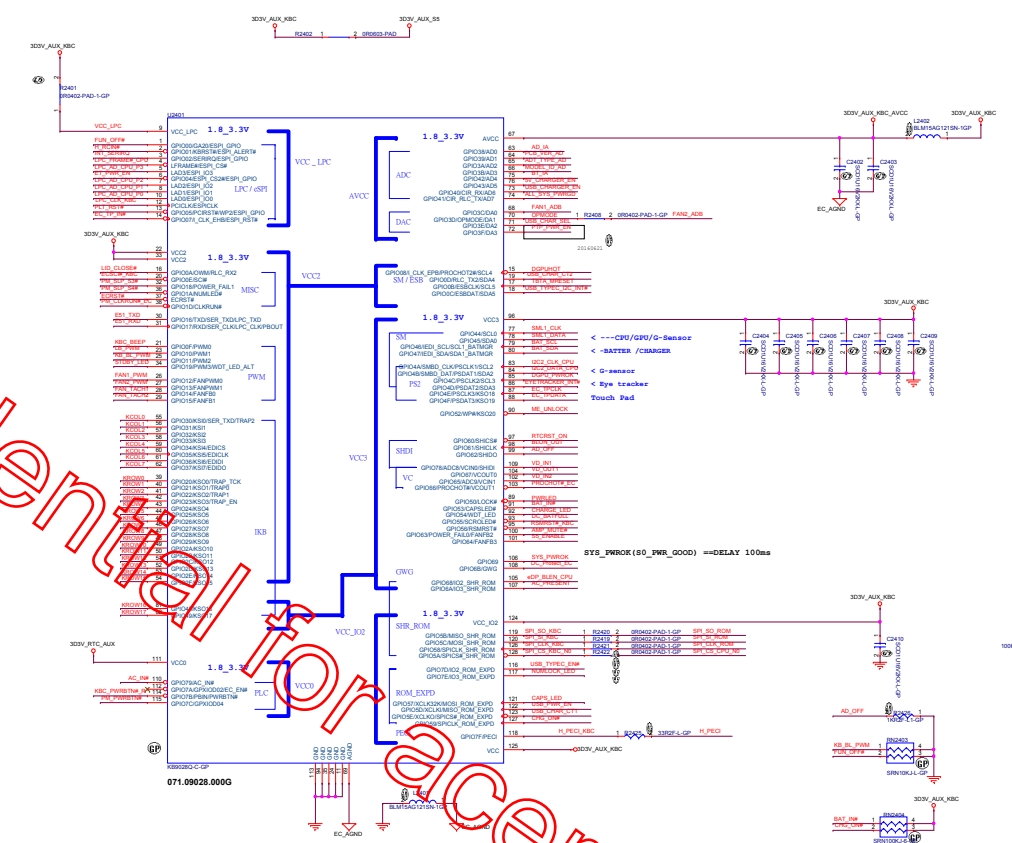


G-sensor
19 SDC2_CLK_CPU
19 SDC2_DATA_CPU
19 SDC2_RST_CPU
38 BT_PWR_EN



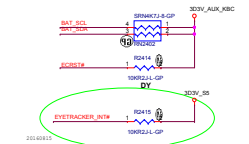
EC_VDD_AUX	Pull Low Register	Pull High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
SA(LAB1)	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V
SB(LAB2)	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V
SC(ENVS)	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V
-1(PD)	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V
-10(MP)	100.0 K	64.9 K	2.011 V	2.017 V	>= 1.894 V
-1M(MP 35 SKV)	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V

AD1_TTYPE_AD	Pull Low Register	Pull High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
65W	NA	100.0 K	3.300 V		>= 3.000 V
90W	100.0 K	NA	0.000 V		< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.684 V
150W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V
150W	64.9 K	100.0 K	1.298 V	1.315 V	>= 1.177 V
180W	76.8 K	100.0 K	1.433 V	1.450 V	>= 1.308 V



OPMODE (Pin70): PU (Default:SPI)
OPMODE(Default/Internal PU):

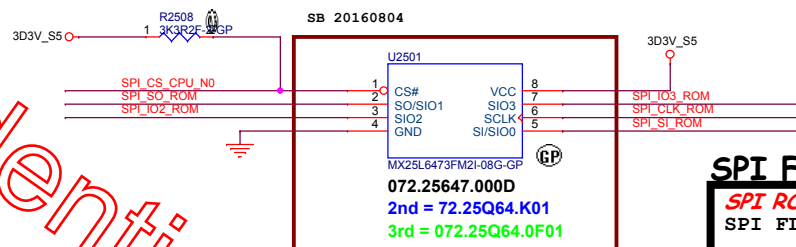
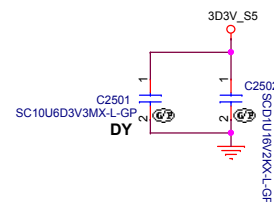
EC9028	AD9 (LAP)
EC9038	DT (MSP)



MODEL	Typical Voltage	Max Voltage	KBC Firmware Setting
Plus (N7C1000)	100.0 K	3.000 V	3.005 V
Plus (N7C1000)	100.0 K	2.750 V	2.759 V
Plus (N7C1000)	100.0 K	2.481 V	2.493 V
Plus (N7C1000)	100.0 K	2.245 V	2.259 V
Plus (N7C1000)	100.0 K	2.011 V	2.017 V
Plus (N7C1000)	100.0 K	1.867 V	1.883 V
Plus (N7C1000)	100.0 K	1.611 V	1.627 V
Plus (N7C1000)	100.0 K	1.365 V	1.381 V
Plus (N7C1000)	100.0 K	1.119 V	1.135 V
Plus (N7C1000)	100.0 K	0.873 V	0.889 V
Plus (N7C1000)	100.0 K	0.627 V	0.643 V
Plus (N7C1000)	100.0 K	0.381 V	0.397 V
Plus (N7C1000)	100.0 K	0.135 V	0.151 V

SSID = Flash.ROM **SPI FLASH ROM (8M byte) for PCH**

SPI FLASH ROM (8M byte) for PCH

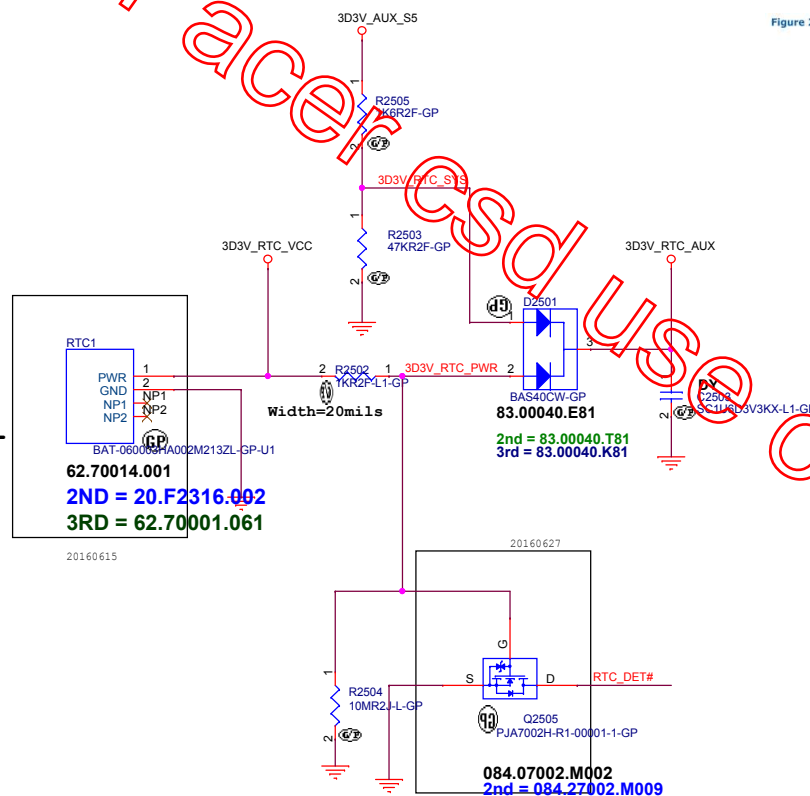


SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil
SPI FLASH ROM (8M byte)

```
1st= 072.25647.000D (MXIC MX25L6473FM2I-08G)
2nd= 72.25Q64.K01 (WINBOND W25Q64FVSSIQ)
3th= 072.25Q64.0F01 (MICRON N25Q064A13ESED0F)
```

Main Func = RTC



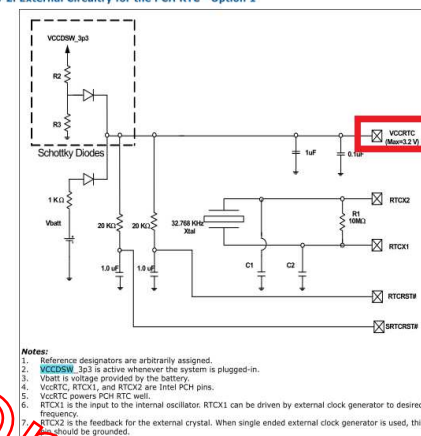
RTC BATTERY

```
1st= 23.20068.001
2nd= 023.20004.0011
```

62.70014.001
2ND = 20.F2316.002
3RD = 62.70001.061

20160615

Figure 28-2. External Circuitry for the PCH RTC - Option 1



Notes:

1. Reference designators are arbitrarily assigned.
2. **VCDCSW**_3p3 is active whenever the system is plugged-in.
3. Vbatt is voltage provided by the battery.
4. VccRTX, RTX1, and RTX2 are Intel PCH pins.
5. VccRTX1 powers PCH RTX well.
6. RTX1 is the input to the internal oscillator. RTX1 can be driven by external clock generator to desired frequency.
7. RTX2 is the feedback for the external crystal. When single ended external clock generator is used, this pin should be grounded.

<Core Design>

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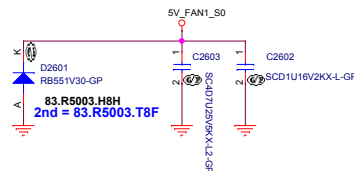
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Flash(KBC+PCH)/RTC
-------	---------------------------

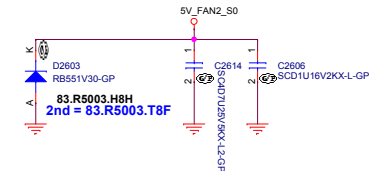
Size A3	Document Number Neptune KLS	Rev -1m
Date: Wednesday, May 17, 2017	Sheet 25 of 105	

SSID = Thermal

Layout 15 mil



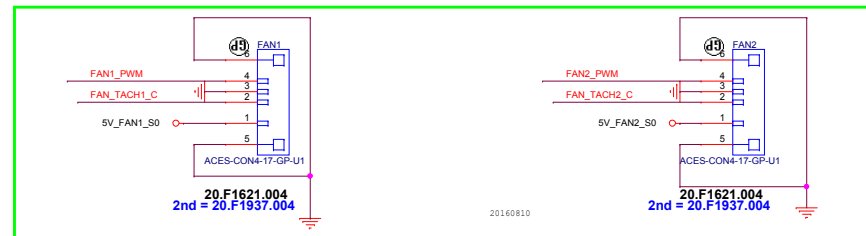
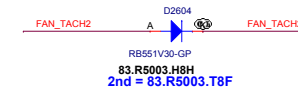
Layout 15 mil



ADB (Active Dusting Blower) function

ADTP TESTPOINT

FAN_TACH1_C 89
FAN_TACH2_C 89



20160810

24 FAN_TACH1 <<<<
24 FAN_TACH2 <<<<

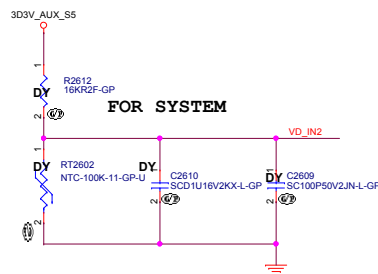
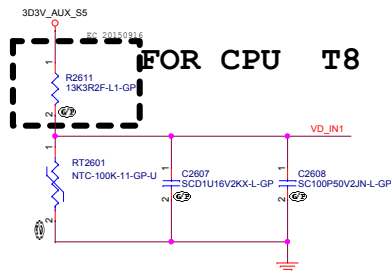
24.89 FAN1_PWM >>>>
24.89 FAN2_PWM >>>>

24 VD_IN1 <<<<
24 VD_IN2 <<<<

24 FAN1_ADB >>>>
24 FAN2_ADB >>>>

24 VD_OUT1 >>>>

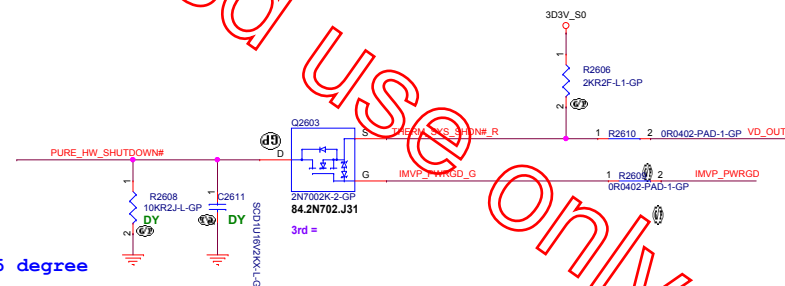
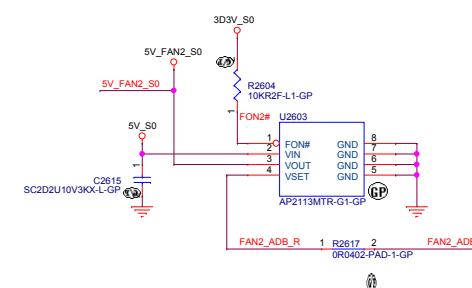
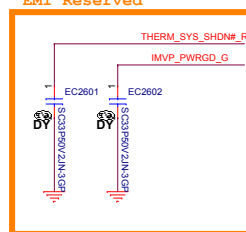
24.40 PURE_HW_SHUTDOWN# <<<<
40.46 IMVP_PWRGD <<<<



FOR SYSTEM

T8 = 85 degree

EMI Reserved



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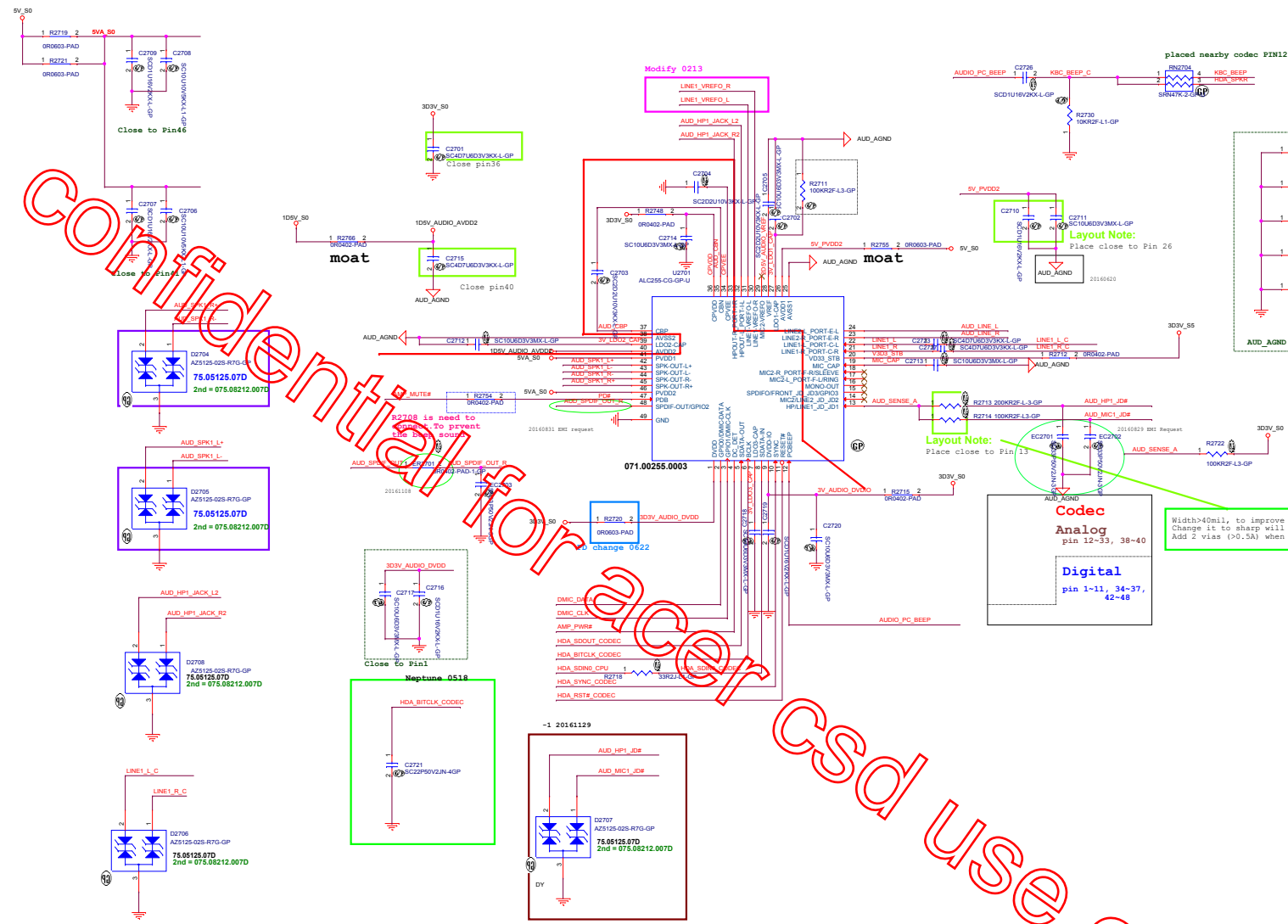
<Core Design>

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File		
Thermal T8 and FAN		
Size	Document Number	Rev
Custom	Neptune KLS	-1m
Date:	Wednesday, May 17, 2017	Sheet 26 of 105




SSID = AUDIO



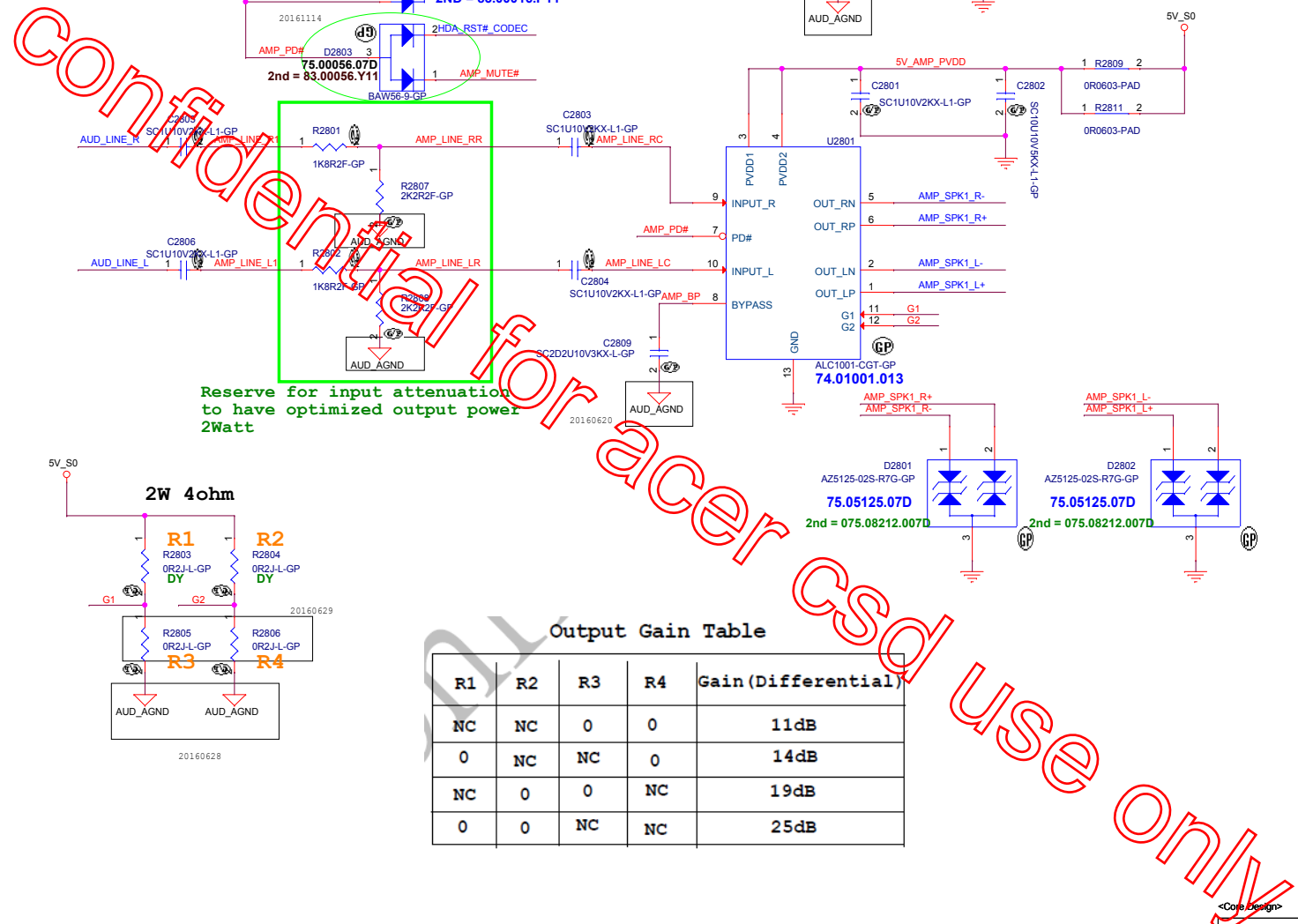
Width>40mil, to improve Headphone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

Codec
Analog
pin 12~33, 38~40

Digital
pin 1~11, 34~37,
42~48

Core Design		 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wb Rd., Hsinshih, Taipei Hsien 221, Taiwan, R.O.C.	
P/N		 Audio Codec ALC255	
Size	Document Number	Rev	
Custom		-1m	
 Neptune KLS			
Date:	Wednesday, May 17, 2017	Sheet	27 of 105

27 AMP_PWR# >>>
 24,27 AMP_MUTE# >>>
 17,27 HDA_RST#_CODEC >>>
 29 AMP_SPK1_R- >>>
 29 AMP_SPK1_R+ >>>
 29 AMP_SPK1_L- >>>
 29 AMP_SPK1_L+ >>>
 27 AUD_LINE_R >>>
 27 AUD_LINE_L >>>

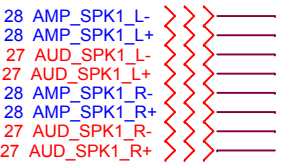
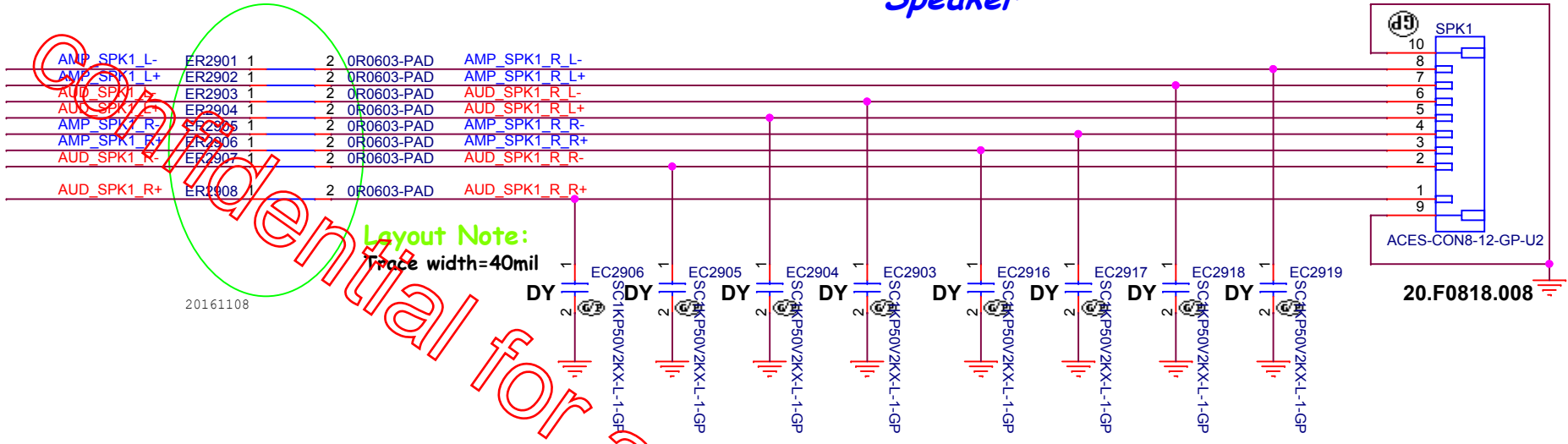


Output Gain Table

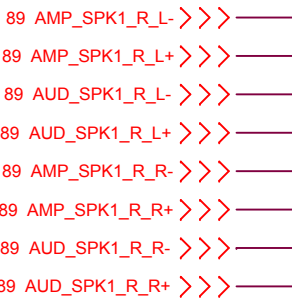
R1	R2	R3	R4	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

SSID = AUDIO

Speaker



AFTP TESTPOINT



<Core Design>

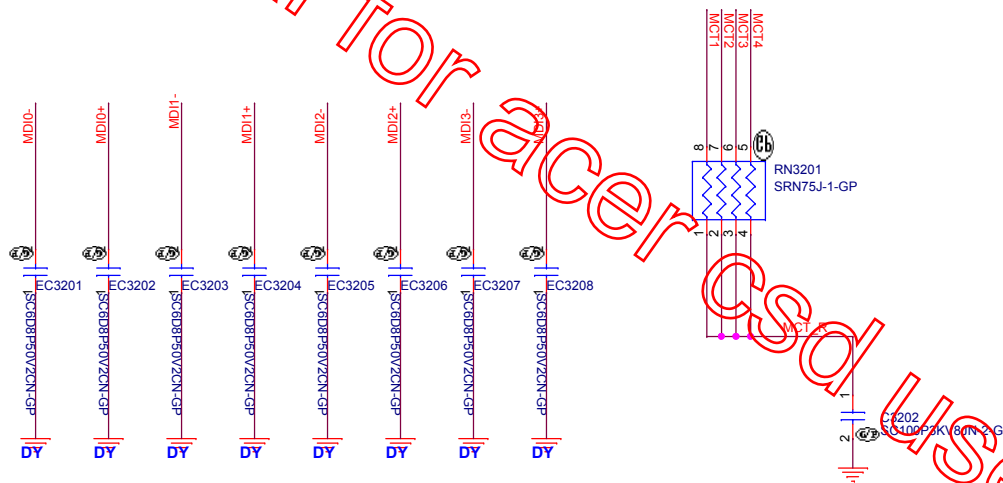
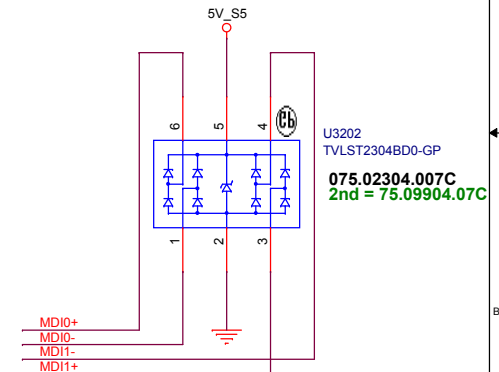
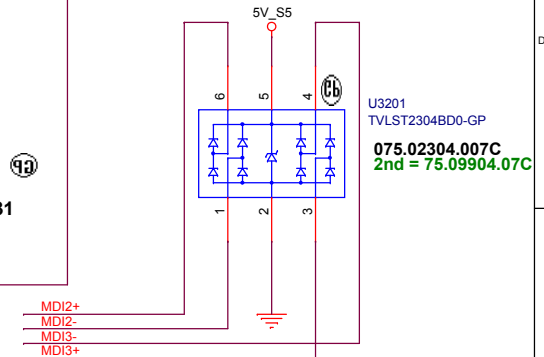
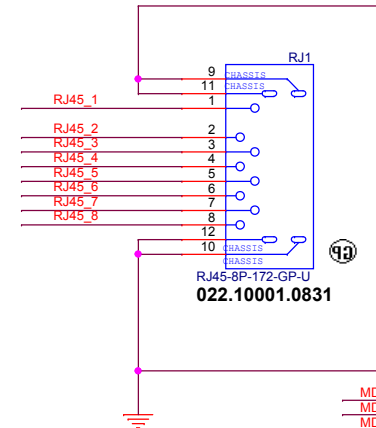
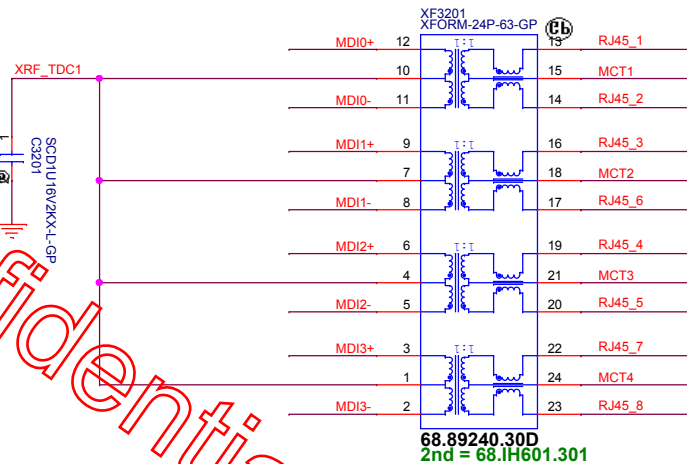
緯創資通		Wistron Corporation	
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Title			
Speaker/ALC255			
Size	Document Number		Rev
A4	Neptune_KLS		-1m
Date:	Wednesday, May 17, 2017	Sheet	29 of 105

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Title (Reserved)			
Size A	Document Number Neptune_KLS		Rev -1m
Date: Wednesday, May 17, 2017		Sheet 30 of	105

SSID = LAN



31.32 MDI0+
31.32 MDI0-
31.32 MDI2-
31.32 MDI2+
31.32 MDI1+
31.32 MDI1-
31.32 MDI3-
31.32 MDI3+

89 RJ45_1
89 RJ45_2
89 RJ45_3
89 RJ45_4
89 RJ45_5
89 RJ45_6
89 RJ45_7
89 RJ45_8

31.32 MDI1+
31.32 MDI1-
31.32 MDI3+
31.32 MDI3-
31.32 MDI0+
31.32 MDI0-
31.32 MDI2+
31.32 MDI2-

<Core Design>

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Title
RJ45+Transformer

Size B Document Number
Neptune_KLS

Date: Wednesday, May 17, 2017

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Rev
-1m

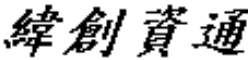
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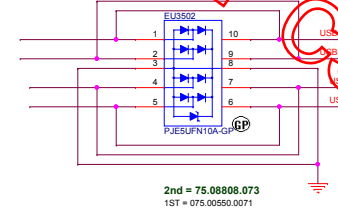
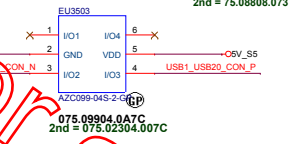
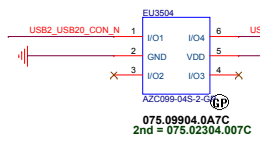
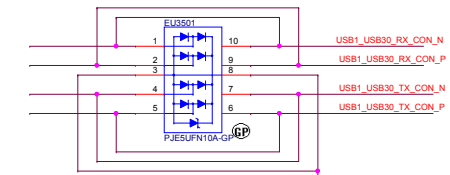
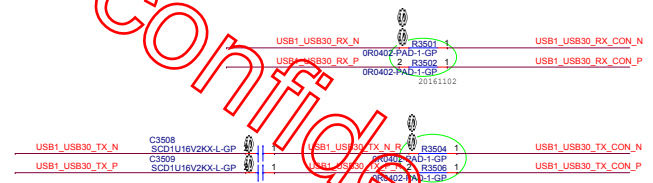
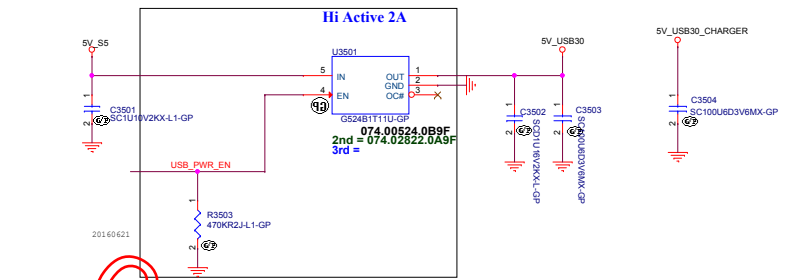
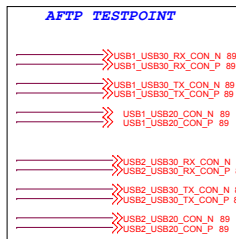
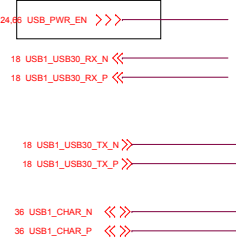
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Title <div>(Reserved)</div>		
Size <div>A</div>	Document Number <div>Neptune_KLS</div>	Rev <div>-1m</div>
Date: Wednesday, May 17, 2017		
Sheet 33 of 105		

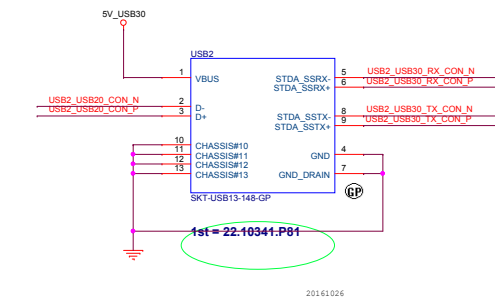
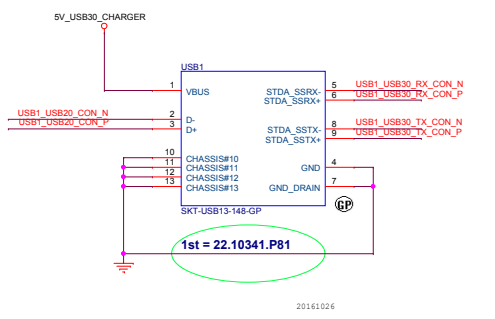
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Title			
CPU CFG CFG STRAP			
Size	Document Number		Rev
A	Neptune_KLS		-1m
Date: Wednesday, May 17, 2017		Sheet 34 of	105



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



24 USB_CHARGER_EN >>>
24 USB_CHAR_SEL >>>

24 USB_CHAR_CT2 >>>

To Connector
35 USB1_CHAR_N <<<
35 USB1_CHAR_P <<<

To PCH
15 USB1_USB20_N <<<
15 USB1_USB20_P <<<

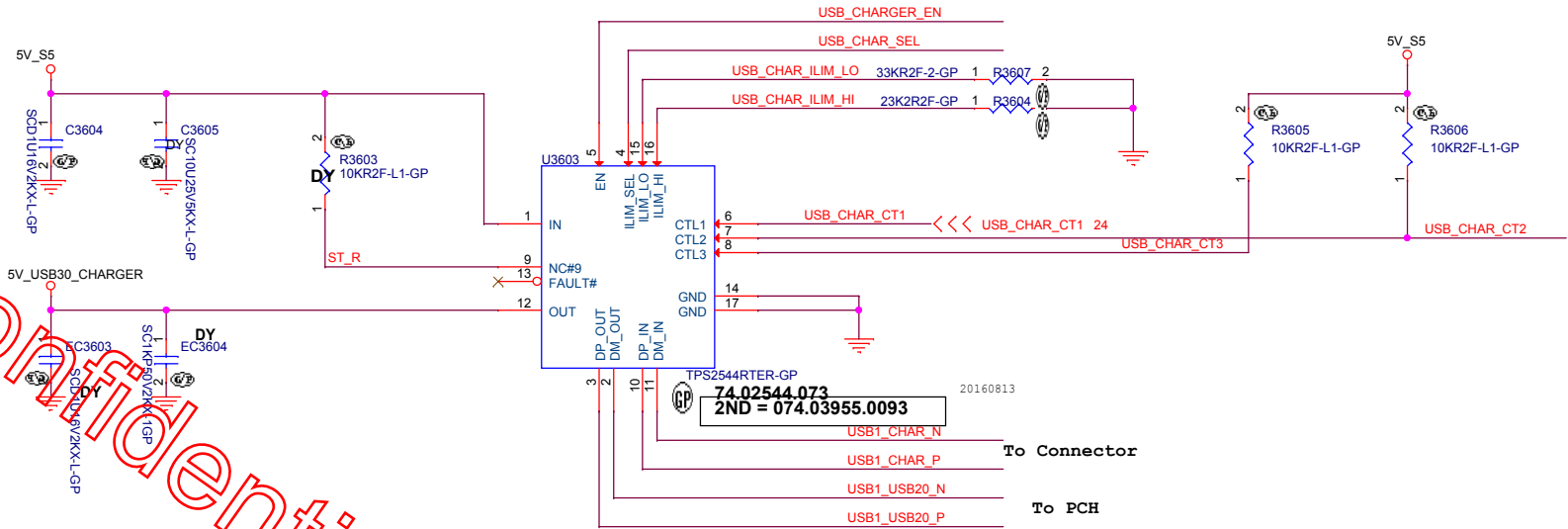


Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Status Output	Notice
0	0	0	0	Discharge	NA	OFF	OLTO held low
0	0	0	1	Discharge	NA	OFF	OLTO held low
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	0	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	Data lines connected
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device forced to stay in DCP BC1.2
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	Charging mode
1	0	1	0	DCP/Divider1	ILIM_LO	OFF	Device forced to stay in DCP divider1
1	0	1	1	DCP/Divider1	ILIM_HI	OFF	Charging mode
1	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
1	1	0	1	SDP1	ILIM_HI	OFF	Data lines connected
1	1	1	0	SDP2	ILIM_LO	OFF	Data lines disconnected
1	1	1	1	CDP	ILIM_HI	CDP	Data lines disconnected Load Detect function active

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Title			
(Reserved)			
Size	Document Number		Rev
A	Neptune_KLS		-1m
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Neptune 0516

Eye-tracker

15 USB5_USB20_N <<>>
15 USB5_USB20_P <<>>
69 SML1_DATA_G <<>>
69 SML1_CLK_G <<>>
19,24,69 EYETRACKER_INT# <<>>
24 ET_PWR_EN <<>>
14 ET_GPIO <<>>

name need talk with SW

14 ET_GPIO <<>>

17 DMIC_CLK_CON_R <<>>

17 DMIC_PCH_DATA <<>>

27 DMIC_CLK <<>>

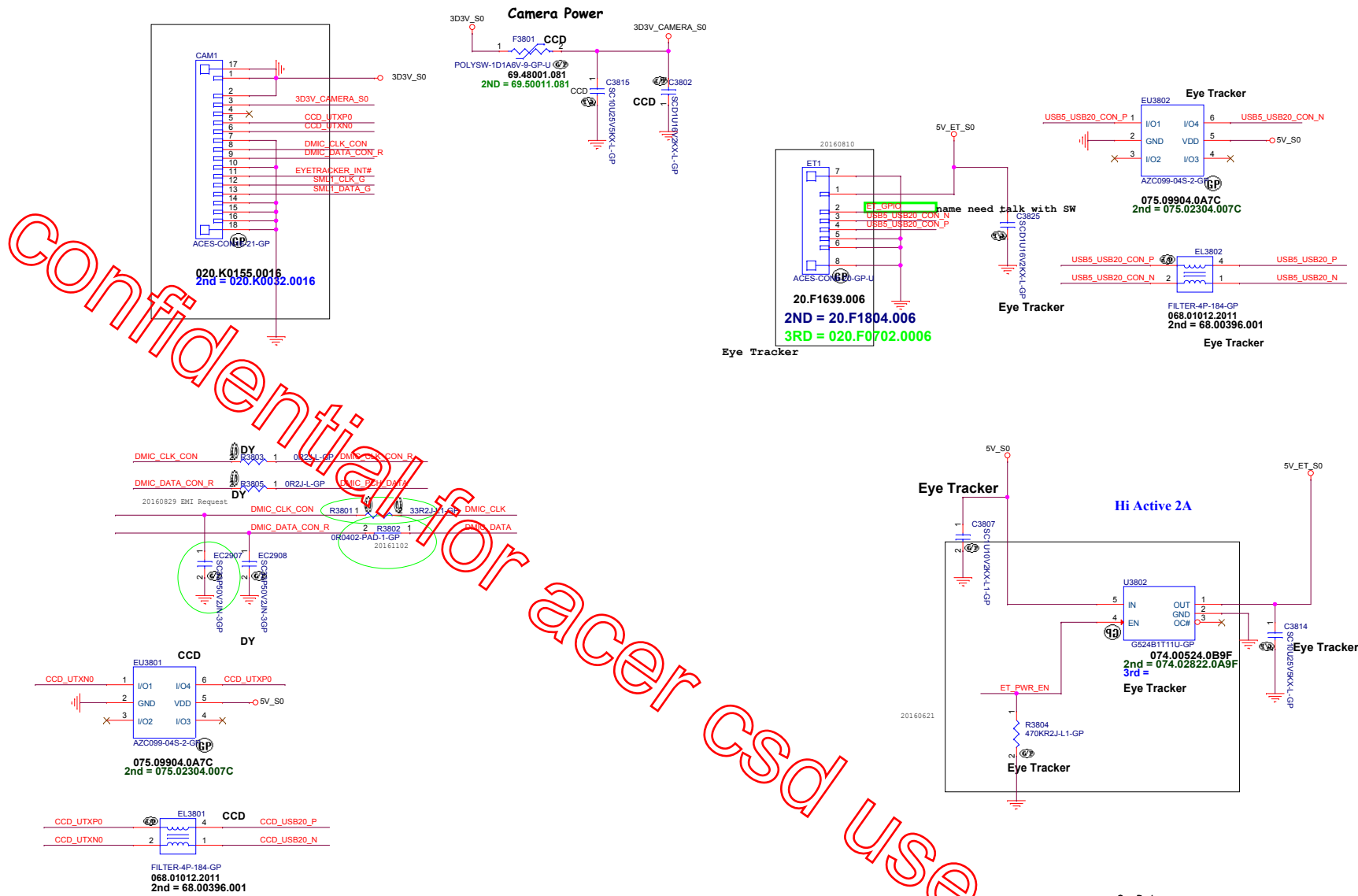
27 DMIC_DATA <<>>

15 CCD_USB20_P <<>>

15 CCD_USB20_N <<>>

AFTP TESTPOINT

<<<< USB5_USB20_CON_N 89
<<<< USB5_USB20_CON_P 89
<<<< CCD_UTXP0 89
<<<< CCD_UTXP0 89
<<<< DMIC_CLK_CON 89
<<<< DMIC_DATA_CON_R 89



<Core Design>

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

File: USB RE DRIVER_3D CAMERA

Size: Document Number
Customer: Neptune KLS
Date: Wednesday, May 17, 2017

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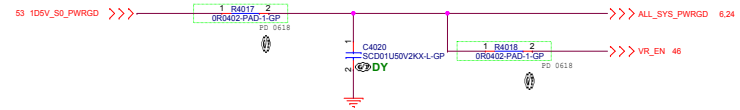
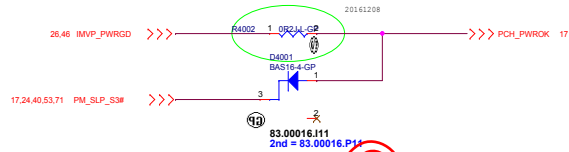
Rev -1m

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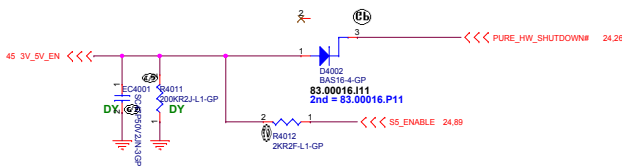
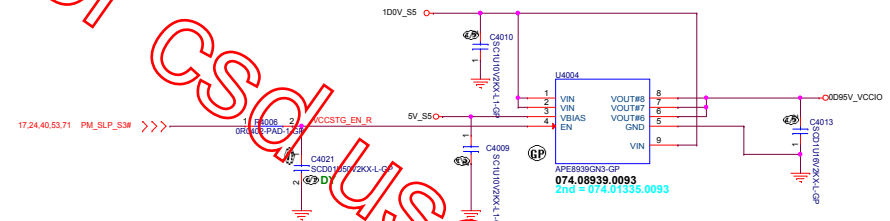
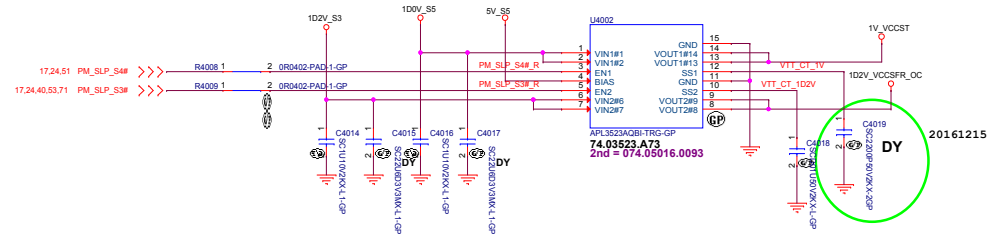
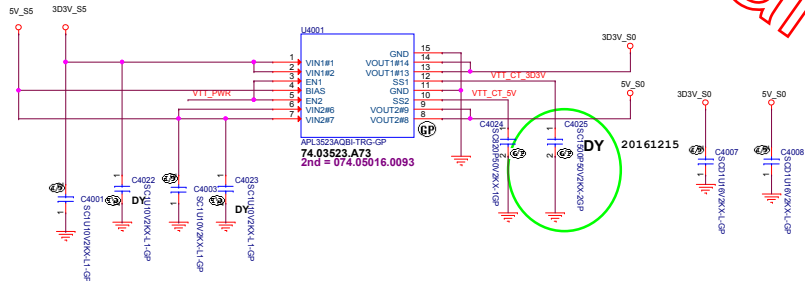
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Power Sequence



ANNIE Run Power



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Power Plane Enable & SEQUENCE
Neptune KLS
Date: Wednesday, May 17, 2017 Sheet 40 of 105

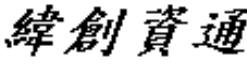
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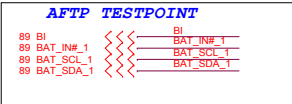
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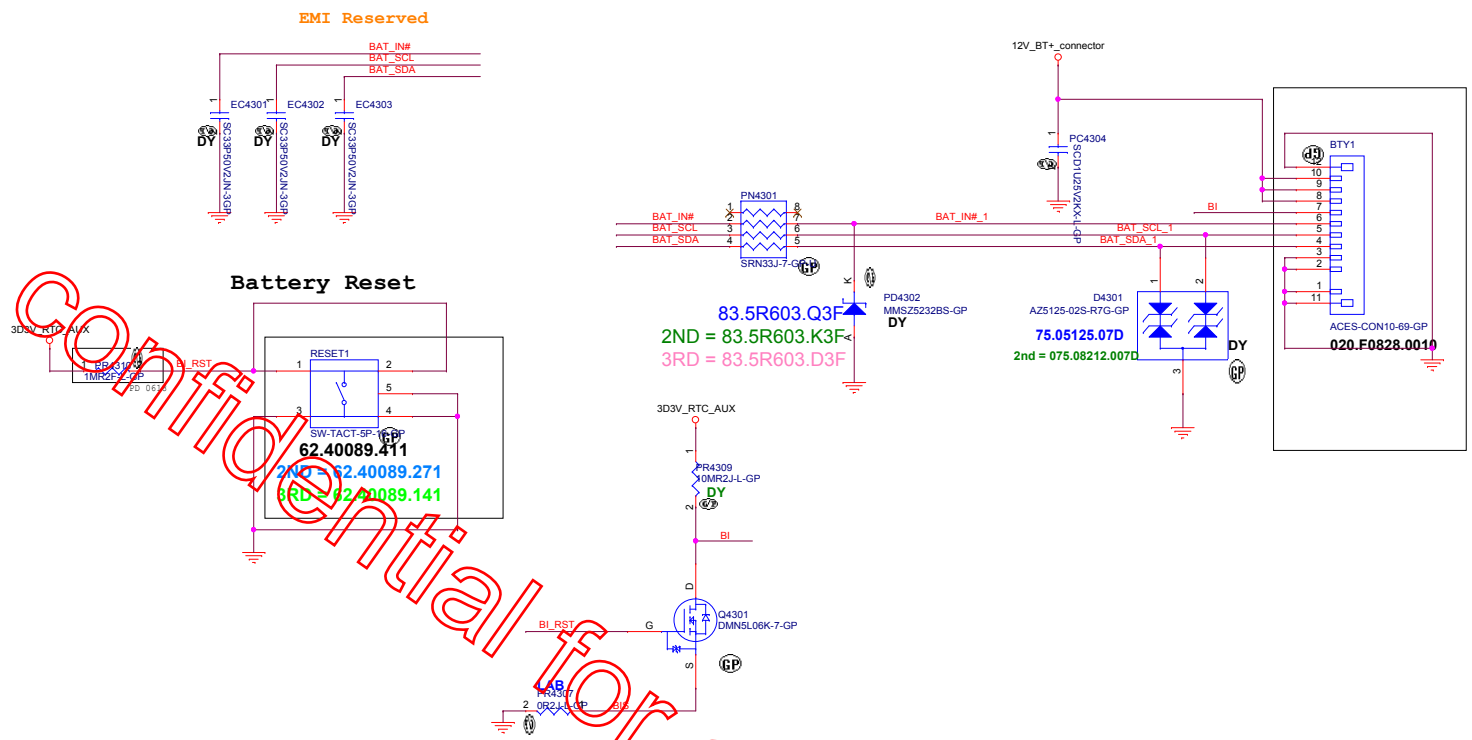
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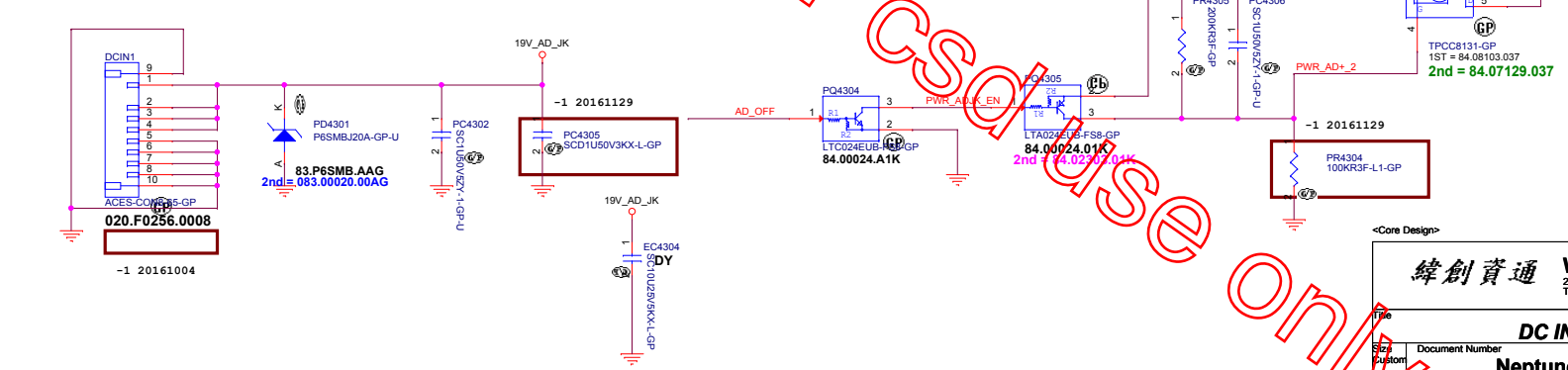


24_AD_OFF >>>



ANNIE solution

Adaptor in to generate DCBATOUT



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File

DC IN / BATT Conn

Rev -1m

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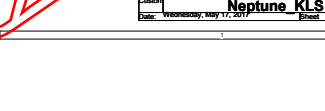
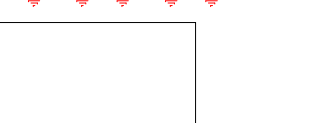
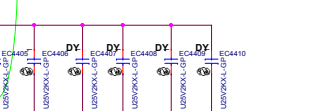
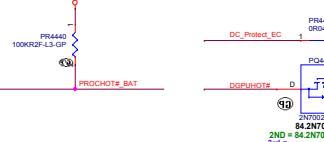
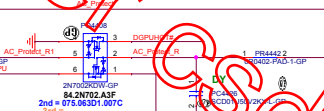
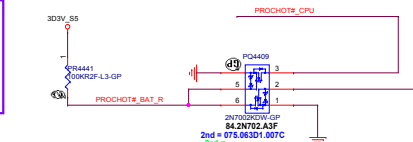
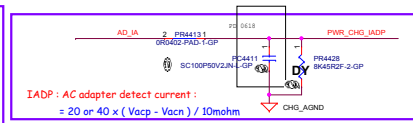
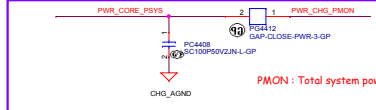
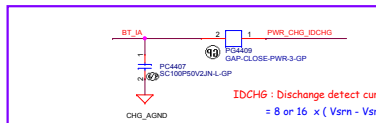
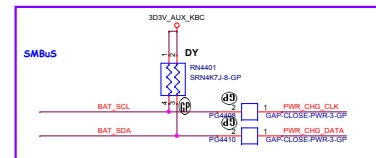
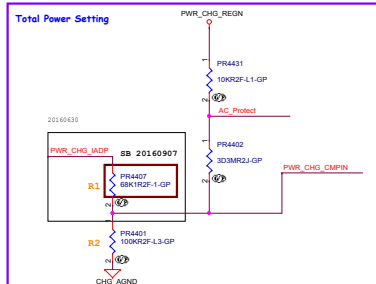
Neptune KLS

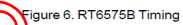
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SSID = Charger

Adaptor			Protect Current	Sense Resistor	Amplifier Ratio	IADP	R1	R2
Watt	Current	Persent					PR4407	PR4407
135.00 W	6.92 A	110%	7.59 A	10 mOhm	20	1.52 V	24.9 K	100 K
180.00 W	9.23 A	110%	10.12 A	10 mOhm	20	2.02 V	68.1 K	100 K

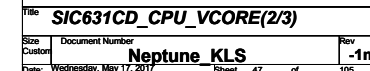




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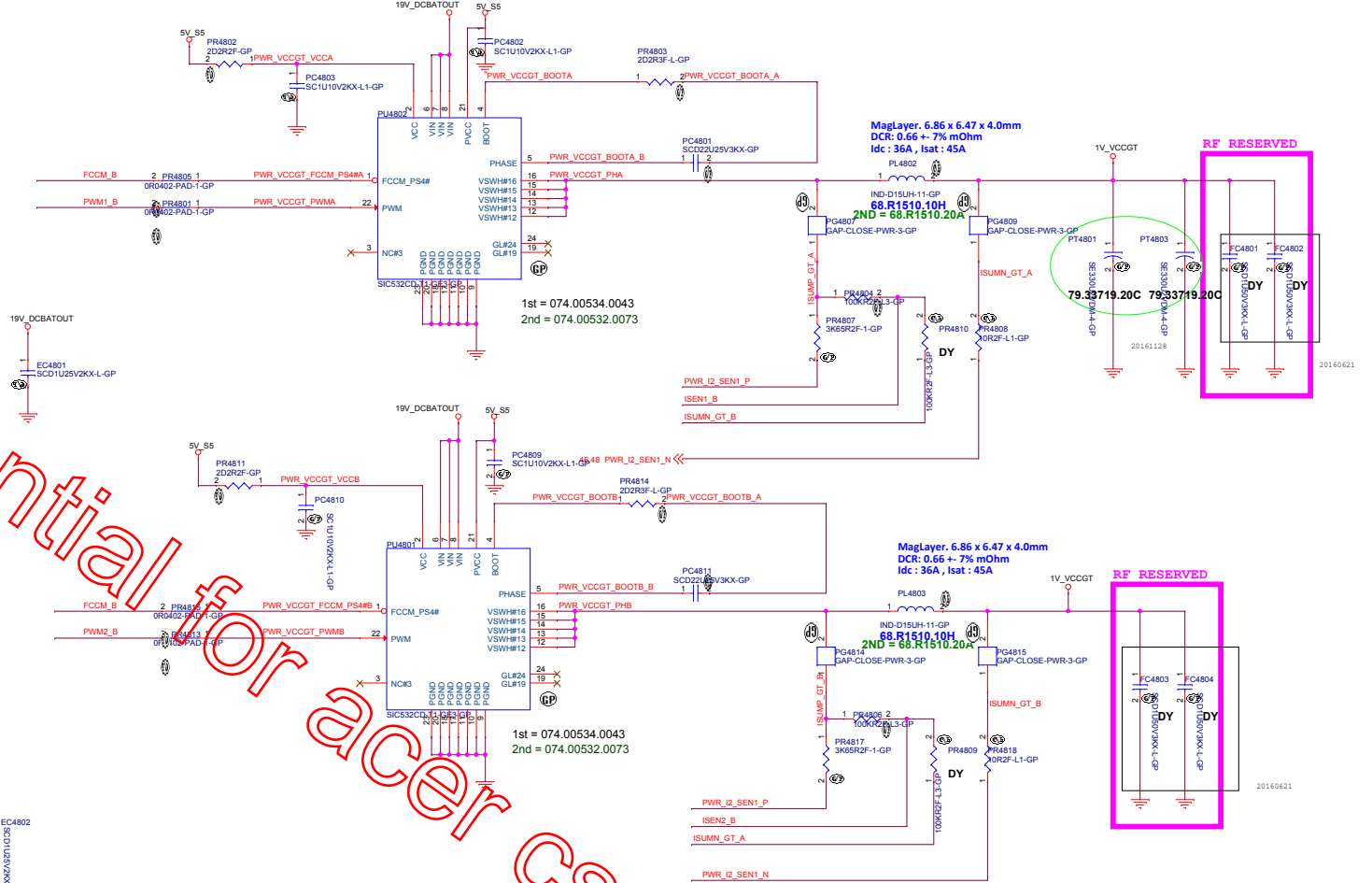
PROG1 - PR4612 : 110K -> VBOOT OV / Slow Rate : 30mV/us / VRA:IA,VR2:GT,VR3:SA
PROG2 - PR4613 : 34K -> VRA IMAX:70A / VRA 2 Phase
PROG3 - PR4614 : 16K9 -> VRB IMAX:50A / VRB 2 Phase
PROG4 - PR4615 : 182K -> Droop Active / VRA & VRB FREQ 750KHz
PROG5 - PR4616 : 121K -> VRC IMAX 13A / VRC FREQ 750KHz

- 26.40 IMVP_PWRGD <<<
- 40 VR_EN >>>
- 50 PWR_H_SEN1_N
- 50 PWR_H_SEN1_P
- 6 VIDOUT_CPU <<<
- 6 VIDALERT1_CPU <<<
- 6 VIDOK_CPU <<<
- 6.24.44 PROCHOT9_CPU <<<
- 44 PWR_CORE_PSYS >>>
- 9 VCGGT_SENSE >>>
- 9 VSSGT_SENSE >>>
- 8 VSSA_SENSE >>>
- 8 VCCA_SENSE >>>
- 48 ISEN1_B >>>
- 48 ISEN2_B >>>
- 48 FCOM_B >>>
- 48 PWM1_B >>>
- 48 PWM2_B >>>
- 48 PWR_I2_SEN1_P >>>
- 48 PWR_I2_SEN1_N >>>
- 47 PWR_I1_SEN1_P >>>
- 47 PWR_I1_SEN1_N >>>
- 7 VSCORE_SENSE >>>
- 7 VCCORE_SENSE >>>



46.48 FCCM_B <<
 46 PWM1_B <<
 46.48 PWR_I2_SEN1_P <<
 46 ISEN1_B <<
 46.48 FCCM_B <<
 46 PWM2_B <<
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 46 ISEN2_B <<
 46.48 PWR_I2_SEN1_N <<

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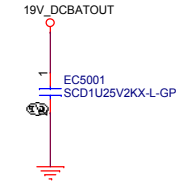
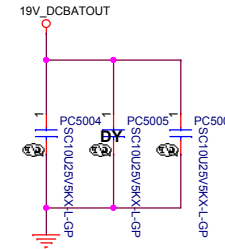
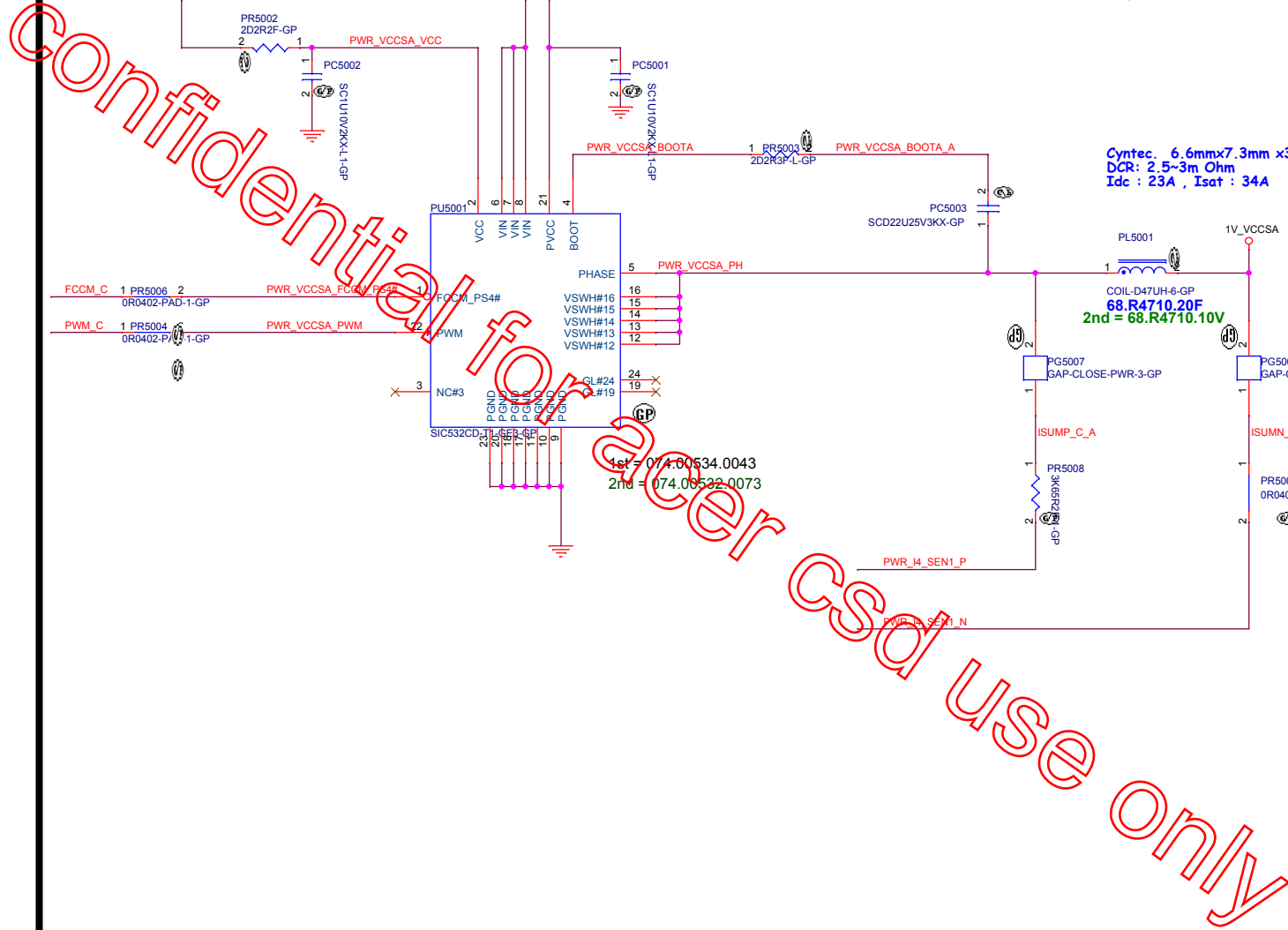


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46 FCCM_C
46 PWM_C
46 PWR_I4_SEN1_P
46 PWR_I4_SEN1_N



Cyntec. 6.6mmx7.3mm x3.0mm
DCR: 2.5~3m Ohm
Idc : 23A , Isat : 34A

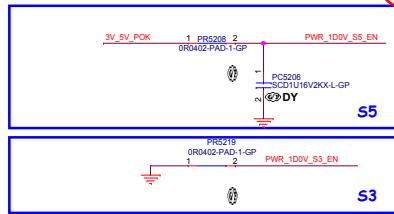
COIL-D47UH-6-GP
68.R4710.20F
2nd = 68.R4710.10V

1st = 074.00534.0043
2nd = 074.00532.0073

17.45_3V_SV_POK

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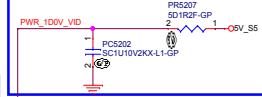
Freq. setting
750K -> 350K Hz



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

OCP setting
78.7K -> OCP 14A

VID
Logic-High = 0.75V
Logic-Low = 0.3V



PWR_100V_VPD

PWR_100V_BOOT

PWR_100V_HG

PWR_100V_PH

PWR_100V_LG

PWR_100V_VDDQ

PWR_100V_FB

PWR_100V_VTTREF

PWR_100V_VTT

PWR_100V_VTTREF

PWR_100V_VTTREF

PWR_100V_VTTREF

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PWR_100V_VTTREF

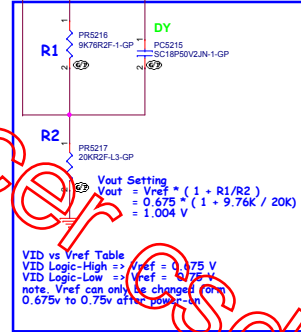
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PWR_100V_VTTREF

PWR_100V_VTTREF

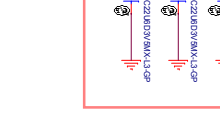
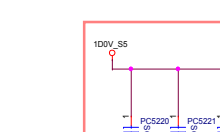
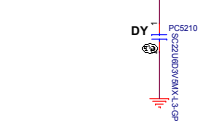
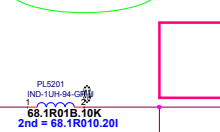
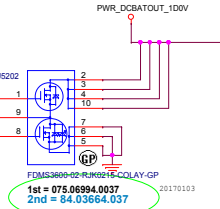
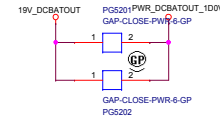
PWR_100V_VTTREF

PWR_100V_VTTREF

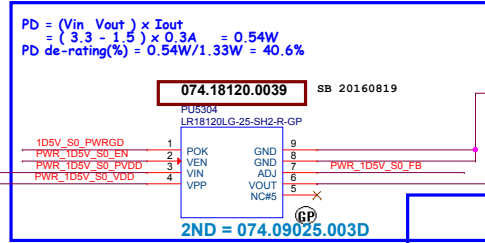
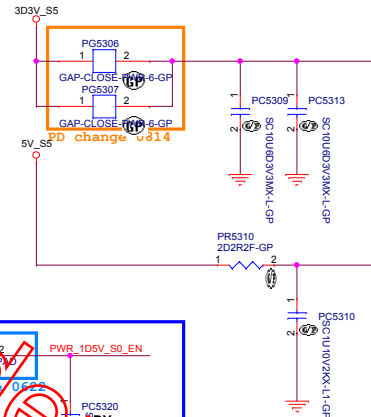


Vout Setting
 $V_{out} = V_{ref} \cdot (1 + R1/R2)$
 $= 0.675 \cdot (1 + 9.76K / 20K)$
 $= 1.004 V$

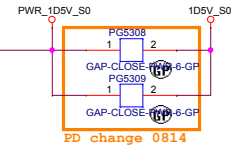
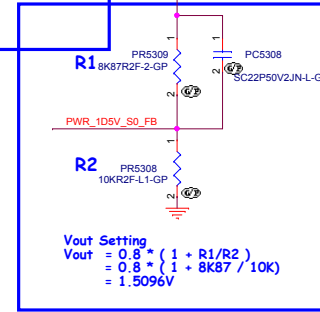
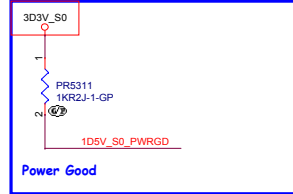
VID vs Vref Table
VID Logic-High => Vref = 0.75 V
VID Logic-Low => Vref = 0.3 V
note: Vref can only be changed from
0.675v to 0.75v after VID = Hi



1D5V_S0



20141028 Jack



Enable
EN_Logi-High = 1.4V
EN_Logi-Low = 0.8V

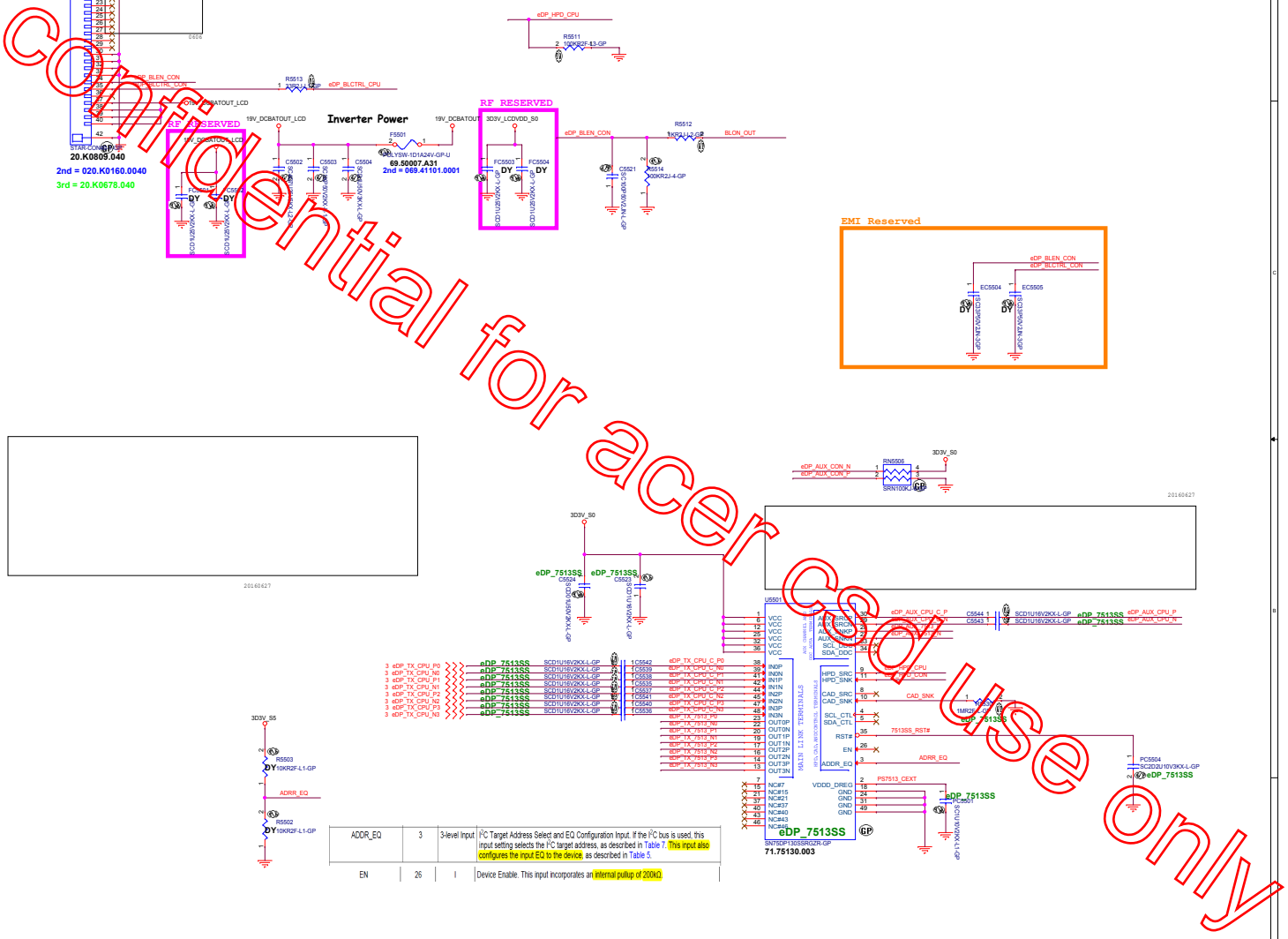
Vout Setting
Vout = $0.8 * (1 + R1/R2)$
Vout = $0.8 * (1 + 8K87 / 10K)$
Vout = 1.5096V

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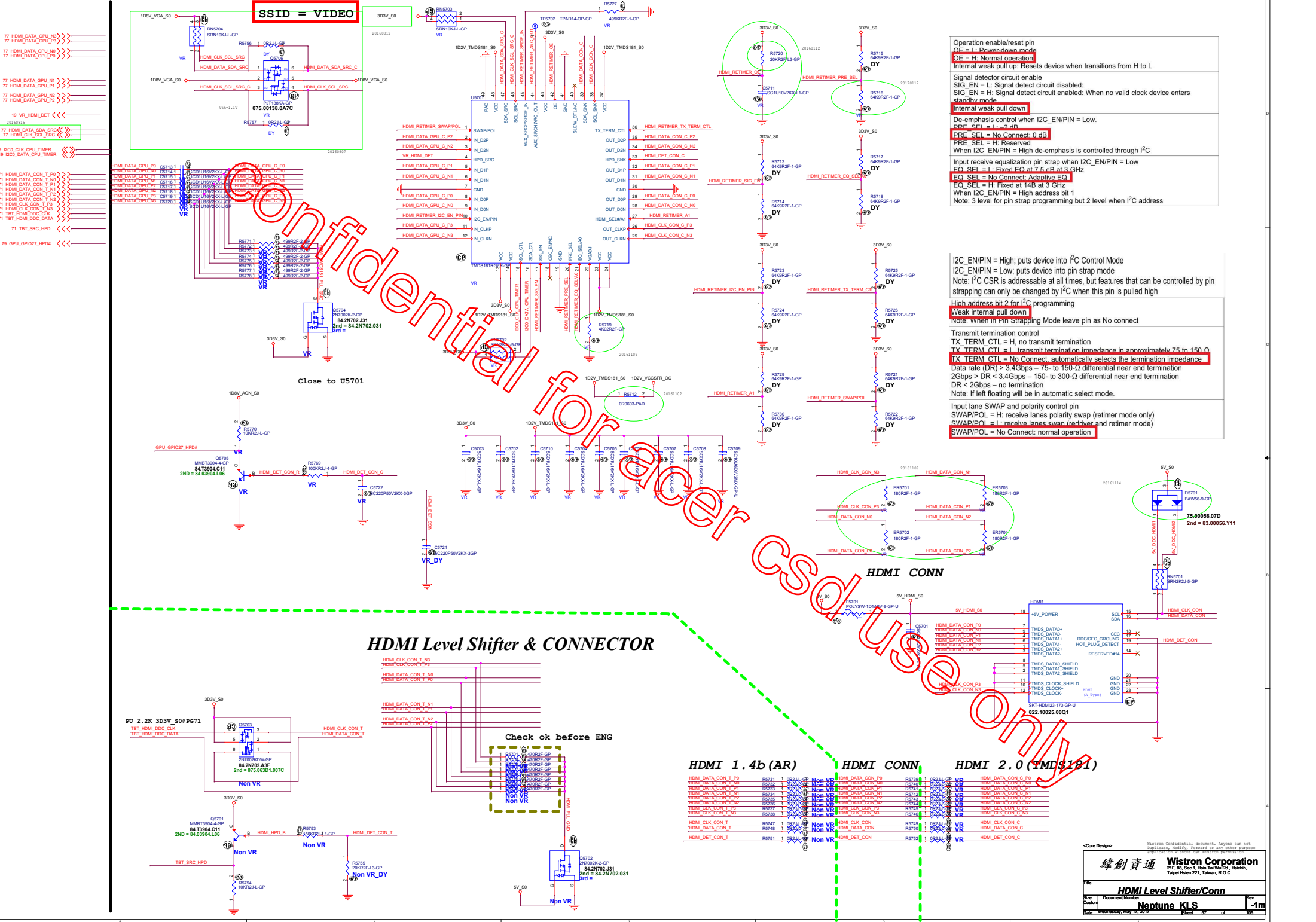
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Size Custom	Document Number	Neptune KLS	Rev -1m
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Operation enable/reset pin
OE = L: Power-down mode
OE = H: Normal operation
Internal weak pull up: Resets device when transitions from H to L

Signal detector circuit enable
SIG_EN = L: Signal detect circuit disabled;
SIG_EN = H: Signal detect circuit enabled: When no valid clock device enters standby mode

Internal weak pull down

De-emphasis control when I2C_EN/PIN = Low:
PRE_SEL = L: 2 dB
PRE_SEL = No Connect: 0 dB
PRE_SEL = H: Reserved
When I2C_EN/PIN = High de-emphasis is controlled through I²C

Input receive equalization pin strap when I2C_EN/PIN = Low
EQ_SEL = L: Fixed EQ at 7.5 dB at 3 GHz
EQ_SEL = No Connect: Adaptive EQ
EQ_SEL = H: Fixed at 148 at 3 GHz
When I2C_EN/PIN = High address bit 1
Note: 3 level for pin strap programming but 2 level when I²C address

I2C_EN/PIN = High: puts device into I²C Control Mode
I2C_EN/PIN = Low: puts device into pin strap mode
Note: I²C CSR is addressable at all times, but features that can be controlled by pin strapping can only be changed by I²C when this pin is pulled high

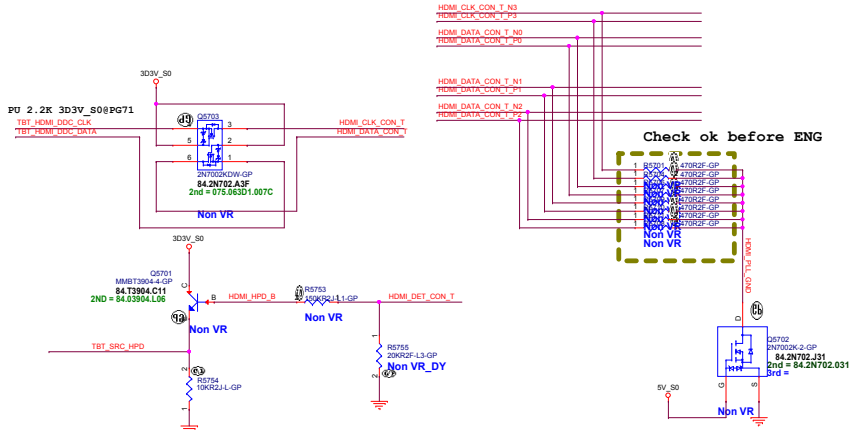
High address bit 2 for I²C programming
Weak internal pull down
Note: when in Pin Strapping Mode leave pin as No connect

Transmit termination control
TX_TERM_CTL = H, no transmit termination
TX_TERM_CTL = L: transmit termination impedance in approximately 75 to 150 Ω
TX_TERM_CTL = No Connect: automatically selects the termination impedance

Data rate (DR) > 3.4Gbps - 75- to 150-Ω differential near end termination
2Gbps > DR < 3.4Gbps - 150- to 300-Ω differential near end termination
DR < 2Gbps - no termination
Note: If left floating will be in automatic select mode.

Input lane SWAP and polarity control pin
SWAP/POL = H: receive lanes polarity swap (retimer mode only)
SWAP/POL = L: receive lanes swap (adriver and retimer mode)
SWAP/POL = No Connect: normal operation

HDMI Level Shifter & CONNECTOR



HDMI 1.4b (AR)	HDMI CONN	HDMI 2.0 (TMD3181)
HDMI DATA CON T P0	R5731 1 092A-L GP	R5730 1 092A-L GP
HDMI DATA CON T P1	R5732 1 092A-L GP	R5731 1 092A-L GP
HDMI DATA CON T P2	R5733 1 092A-L GP	R5732 1 092A-L GP
HDMI DATA CON T P3	R5734 1 092A-L GP	R5733 1 092A-L GP
HDMI DATA CON T P4	R5735 1 092A-L GP	R5734 1 092A-L GP
HDMI DATA CON T P5	R5736 1 092A-L GP	R5735 1 092A-L GP
HDMI DATA CON T P6	R5737 1 092A-L GP	R5736 1 092A-L GP
HDMI DATA CON T P7	R5738 1 092A-L GP	R5737 1 092A-L GP
HDMI DATA CON T P8	R5739 1 092A-L GP	R5738 1 092A-L GP
HDMI DATA CON T P9	R5740 1 092A-L GP	R5739 1 092A-L GP
HDMI DATA CON T P10	R5741 1 092A-L GP	R5740 1 092A-L GP
HDMI DATA CON T P11	R5742 1 092A-L GP	R5741 1 092A-L GP
HDMI DATA CON T P12	R5743 1 092A-L GP	R5742 1 092A-L GP
HDMI DATA CON T P13	R5744 1 092A-L GP	R5743 1 092A-L GP
HDMI DATA CON T P14	R5745 1 092A-L GP	R5744 1 092A-L GP
HDMI DATA CON T P15	R5746 1 092A-L GP	R5745 1 092A-L GP
HDMI DATA CON T P16	R5747 1 092A-L GP	R5746 1 092A-L GP
HDMI DATA CON T P17	R5748 1 092A-L GP	R5747 1 092A-L GP
HDMI DATA CON T P18	R5749 1 092A-L GP	R5748 1 092A-L GP
HDMI DATA CON T P19	R5750 1 092A-L GP	R5749 1 092A-L GP
HDMI DATA CON T P20	R5751 1 092A-L GP	R5750 1 092A-L GP
HDMI DATA CON T P21	R5752 1 092A-L GP	R5751 1 092A-L GP
HDMI DATA CON T P22	R5753 1 092A-L GP	R5752 1 092A-L GP
HDMI DATA CON T P23	R5754 1 092A-L GP	R5753 1 092A-L GP
HDMI DATA CON T P24	R5755 1 092A-L GP	R5754 1 092A-L GP
HDMI DATA CON T P25	R5756 1 092A-L GP	R5755 1 092A-L GP
HDMI DATA CON T P26	R5757 1 092A-L GP	R5756 1 092A-L GP
HDMI DATA CON T P27	R5758 1 092A-L GP	R5757 1 092A-L GP
HDMI DATA CON T P28	R5759 1 092A-L GP	R5758 1 092A-L GP
HDMI DATA CON T P29	R5760 1 092A-L GP	R5759 1 092A-L GP
HDMI DATA CON T P30	R5761 1 092A-L GP	R5760 1 092A-L GP
HDMI DATA CON T P31	R5762 1 092A-L GP	R5761 1 092A-L GP
HDMI DATA CON T P32	R5763 1 092A-L GP	R5762 1 092A-L GP
HDMI DATA CON T P33	R5764 1 092A-L GP	R5763 1 092A-L GP
HDMI DATA CON T P34	R5765 1 092A-L GP	R5764 1 092A-L GP
HDMI DATA CON T P35	R5766 1 092A-L GP	R5765 1 092A-L GP
HDMI DATA CON T P36	R5767 1 092A-L GP	R5766 1 092A-L GP
HDMI DATA CON T P37	R5768 1 092A-L GP	R5767 1 092A-L GP
HDMI DATA CON T P38	R5769 1 092A-L GP	R5768 1 092A-L GP
HDMI DATA CON T P39	R5770 1 092A-L GP	R5769 1 092A-L GP
HDMI DATA CON T P40	R5771 1 092A-L GP	R5770 1 092A-L GP
HDMI DATA CON T P41	R5772 1 092A-L GP	R5771 1 092A-L GP
HDMI DATA CON T P42	R5773 1 092A-L GP	R5772 1 092A-L GP
HDMI DATA CON T P43	R5774 1 092A-L GP	R5773 1 092A-L GP
HDMI DATA CON T P44	R5775 1 092A-L GP	R5774 1 092A-L GP
HDMI DATA CON T P45	R5776 1 092A-L GP	R5775 1 092A-L GP
HDMI DATA CON T P46	R5777 1 092A-L GP	R5776 1 092A-L GP
HDMI DATA CON T P47	R5778 1 092A-L GP	R5777 1 092A-L GP
HDMI DATA CON T P48	R5779 1 092A-L GP	R5778 1 092A-L GP
HDMI DATA CON T P49	R5780 1 092A-L GP	R5779 1 092A-L GP
HDMI DATA CON T P50	R5781 1 092A-L GP	R5780 1 092A-L GP
HDMI DATA CON T P51	R5782 1 092A-L GP	R5781 1 092A-L GP
HDMI DATA CON T P52	R5783 1 092A-L GP	R5782 1 092A-L GP
HDMI DATA CON T P53	R5784 1 092A-L GP	R5783 1 092A-L GP
HDMI DATA CON T P54	R5785 1 092A-L GP	R5784 1 092A-L GP
HDMI DATA CON T P55	R5786 1 092A-L GP	R5785 1 092A-L GP
HDMI DATA CON T P56	R5787 1 092A-L GP	R5786 1 092A-L GP
HDMI DATA CON T P57	R5788 1 092A-L GP	R5787 1 092A-L GP
HDMI DATA CON T P58	R5789 1 092A-L GP	R5788 1 092A-L GP
HDMI DATA CON T P59	R5790 1 092A-L GP	R5789 1 092A-L GP
HDMI DATA CON T P60	R5791 1 092A-L GP	R5790 1 092A-L GP
HDMI DATA CON T P61	R5792 1 092A-L GP	R5791 1 092A-L GP
HDMI DATA CON T P62	R5793 1 092A-L GP	R5792 1 092A-L GP
HDMI DATA CON T P63	R5794 1 092A-L GP	R5793 1 092A-L GP
HDMI DATA CON T P64	R5795 1 092A-L GP	R5794 1 092A-L GP
HDMI DATA CON T P65	R5796 1 092A-L GP	R5795 1 092A-L GP
HDMI DATA CON T P66	R5797 1 092A-L GP	R5796 1 092A-L GP
HDMI DATA CON T P67	R5798 1 092A-L GP	R5797 1 092A-L GP
HDMI DATA CON T P68	R5799 1 092A-L GP	R5798 1 092A-L GP
HDMI DATA CON T P69	R5800 1 092A-L GP	R5799 1 092A-L GP
HDMI DATA CON T P70	R5801 1 092A-L GP	R5800 1 092A-L GP
HDMI DATA CON T P71	R5802 1 092A-L GP	R5801 1 092A-L GP
HDMI DATA CON T P72	R5803 1 092A-L GP	R5802 1 092A-L GP
HDMI DATA CON T P73	R5804 1 092A-L GP	R5803 1 092A-L GP
HDMI DATA CON T P74	R5805 1 092A-L GP	R5804 1 092A-L GP
HDMI DATA CON T P75	R5806 1 092A-L GP	R5805 1 092A-L GP
HDMI DATA CON T P76	R5807 1 092A-L GP	R5806 1 092A-L GP
HDMI DATA CON T P77	R5808 1 092A-L GP	R5807 1 092A-L GP
HDMI DATA CON T P78	R5809 1 092A-L GP	R5808 1 092A-L GP
HDMI DATA CON T P79	R5810 1 092A-L GP	R5809 1 092A-L GP
HDMI DATA CON T P80	R5811 1 092A-L GP	R5810 1 092A-L GP
HDMI DATA CON T P81	R5812 1 092A-L GP	R5811 1 092A-L GP
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HDMI DATA CON T P84	R5815 1 092A-L GP	R5814 1 092A-L GP
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HDMI DATA CON T P89	R5820 1 092A-L GP	R5819 1 092A-L GP
HDMI DATA CON T P90	R5821 1 092A-L GP	R5820 1 092A-L GP
HDMI DATA CON T P91	R5822 1 092A-L GP	R5821 1 092A-L GP
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HDMI DATA CON T P93	R5824 1 092A-L GP	R5823 1 092A-L GP
HDMI DATA CON T P94	R5825 1 092A-L GP	R5824 1 092A-L GP
HDMI DATA CON T P95	R5826 1 092A-L GP	R5825 1 092A-L GP
HDMI DATA CON T P96	R5827 1 092A-L GP	R5826 1 092A-L GP
HDMI DATA CON T P97	R5828 1 092A-L GP	R5827 1 092A-L GP
HDMI DATA CON T P98	R5829 1 092A-L GP	R5828 1 092A-L GP
HDMI DATA CON T P99	R5830 1 092A-L GP	R5829 1 092A-L GP
HDMI DATA CON T P100	R5831 1 092A-L GP	R5830 1 092A-L GP

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Title <div>(Reserved)</div>		
Size A	Document Number <div>Neptune_KLS</div>	Rev <div>-1m</div>
Date: Wednesday, May 17, 2017		Sheet 58 of 105

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Title (Reserved)			
Size A	Document Number Neptune_KLS		Rev -1m
Date: Wednesday, May 17, 2017		Sheet 59 of	105

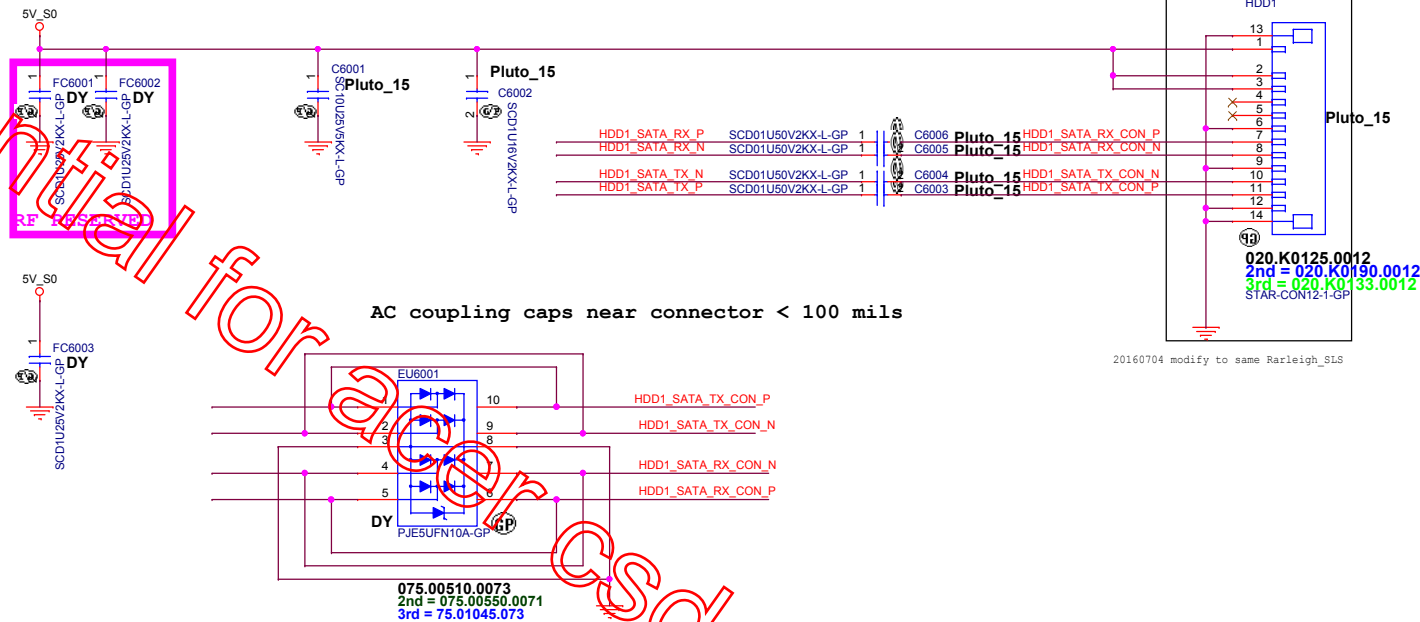
16 HDD1_SATA_RX_N >>>=====
16 HDD1_SATA_RX_P <<<=====
16 HDD1_SATA_TX_N >>>=====
16 HDD1_SATA_TX_P <<<=====

SSID = SATA

SATA HDD1 Connector

AFTP TESTPOINT

89 HDD1_SATA_TX_CON_P >>>=====
89 HDD1_SATA_TX_CON_N <<<=====
89 HDD1_SATA_RX_CON_P >>>=====
89 HDD1_SATA_RX_CON_N <<<=====



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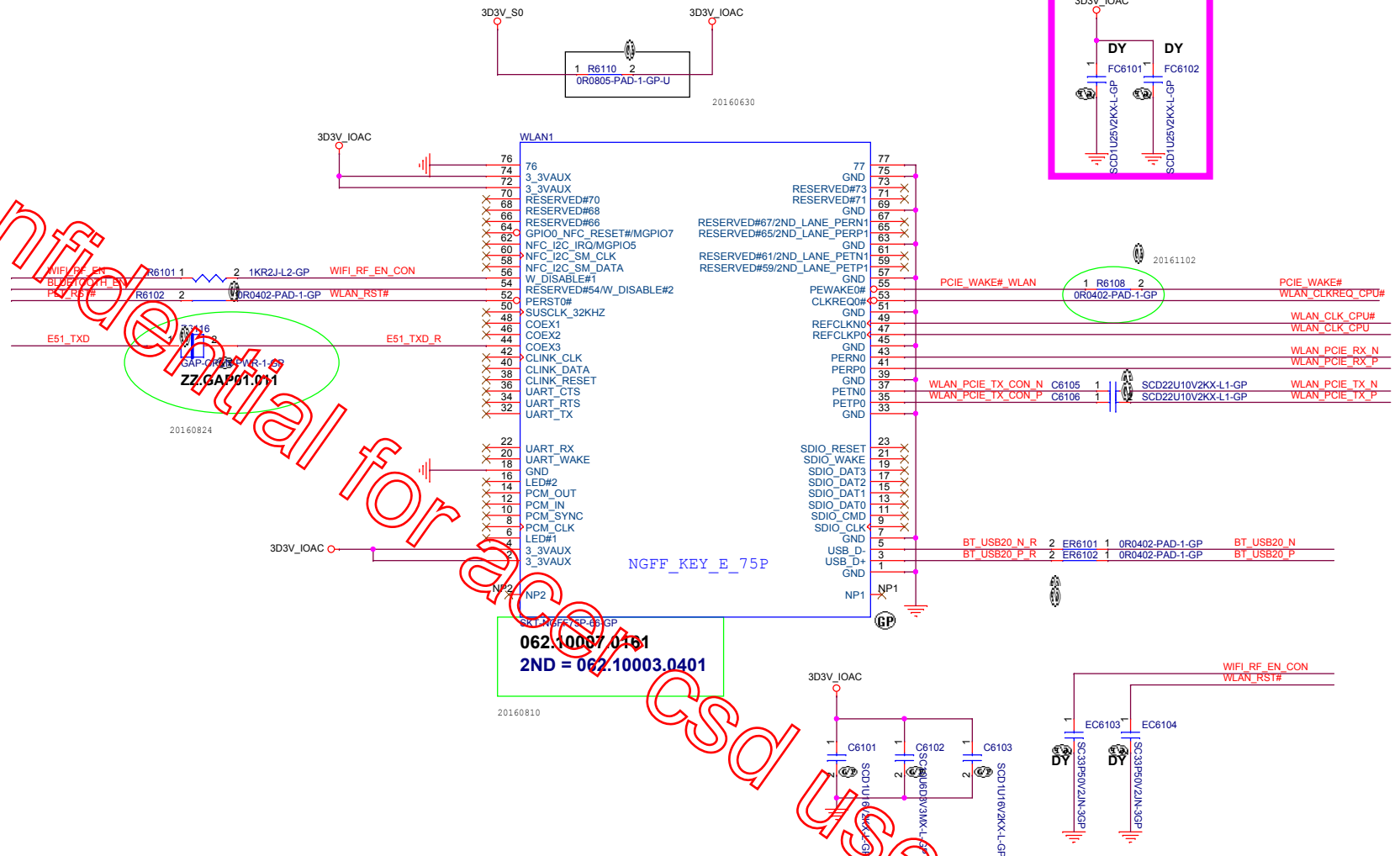
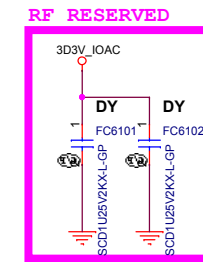
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Title			HDD/ODD	
Size	Document Number	Rev		
Custom	Neptune KLS	-1m		
Date:	Wednesday, May 17, 2017	Sheet	60	of 105

NGFF Connector (802.11a/b/g/n)



```

>>> PCIE_WAKE# WLAN 89
WLAN_CLK_KREQ_CPU# 18,61,89
<<< WLAN_CLK_CPU# 18,61,89
WLAN_CLK_CPU 18,61,89
>>> WLAN_PCIE_RX_N 15,61,89
WLAN_PCIE_RX_P 15,61,89
<<< WLAN_PCIE_TX_CON_N 89
WLAN_PCIE_TX_CON_P 89
<<<
>>> BT_USB20_N_R 89
BT_USB20_P_R 89
<<<
>>> WIFI_RF_EN_CON 89
BLUETOOTH_EN 19,61,89
WLAN_RST# 89
<<<
<<< E51_TXD_R 89

```

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Mini card-WLAN

Size

	Document Number
--	-----------------

Neptune KLS

Date: Wednesday, May 17, 2017

Sheet 61

Rev

-1m

105

SSID = Wireless

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Title (Reserved)WWAN			
Size A	Document Number Neptune_KLS		Rev -1m
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Mini Card Connector (NGFF m-SATA)

Notes:

- Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the SATA Tx and Rx channel support 10 Gbps. However, the 10 nF capacitor on Rx can be removed if DC coupled DODs / devices are NOT used.
- Design Constraint: For PCIe® Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **this option DOES NOT support DC coupled DODs / Devices.**
- Design Constraint: For PCIe® Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO capacitor is required for motherboard Rx channel. **this option DOES NOT support DC coupled DODs / Devices.**
- Design Constraints, Required: Refer to the Chapter 3, "General Differential Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.

Filter	Reset	USD Pin-Out (Mechanical)
1	NC	NC
2	NC	NC
3	NC	NC
4	NC	NC
5	NC	NC
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10	NC	NC
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132	NC	NC
133	NC	NC
134	NC	NC
135	NC	NC
136	NC	NC
137	NC	NC
138	NC	NC
139	NC	

							
<p>~Data Design~</p>		<p>Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wai Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.</p>					
<p>華創資通</p>							
<p>S5D-NGFF</p>							
<p>Neptune KLS</p>							
Size	Document No.						Rev
X2							-1
Y2	Wednesday, May 1, 2002	12:00 PM	100%	100%	100%	100%	100%

20161031

LB1

5

1

2 LB_PWM_LED1

3 LB_PWM_LED2

4

6

GP

ACES-CON4-29-GP

20.F1639.004

2ND = 020.F0700.0004

3RD = 20.F1804.004

R6401 1

R6402 1

180R2F-1-GP

200R2F-L-GP

LB_PWM_R

D

G

S

1

C6401

SCD1U16V2KX-

LB_PWM

Power Button

3

6

1

2

5

PW1

SW-TACT-4P-59-GP

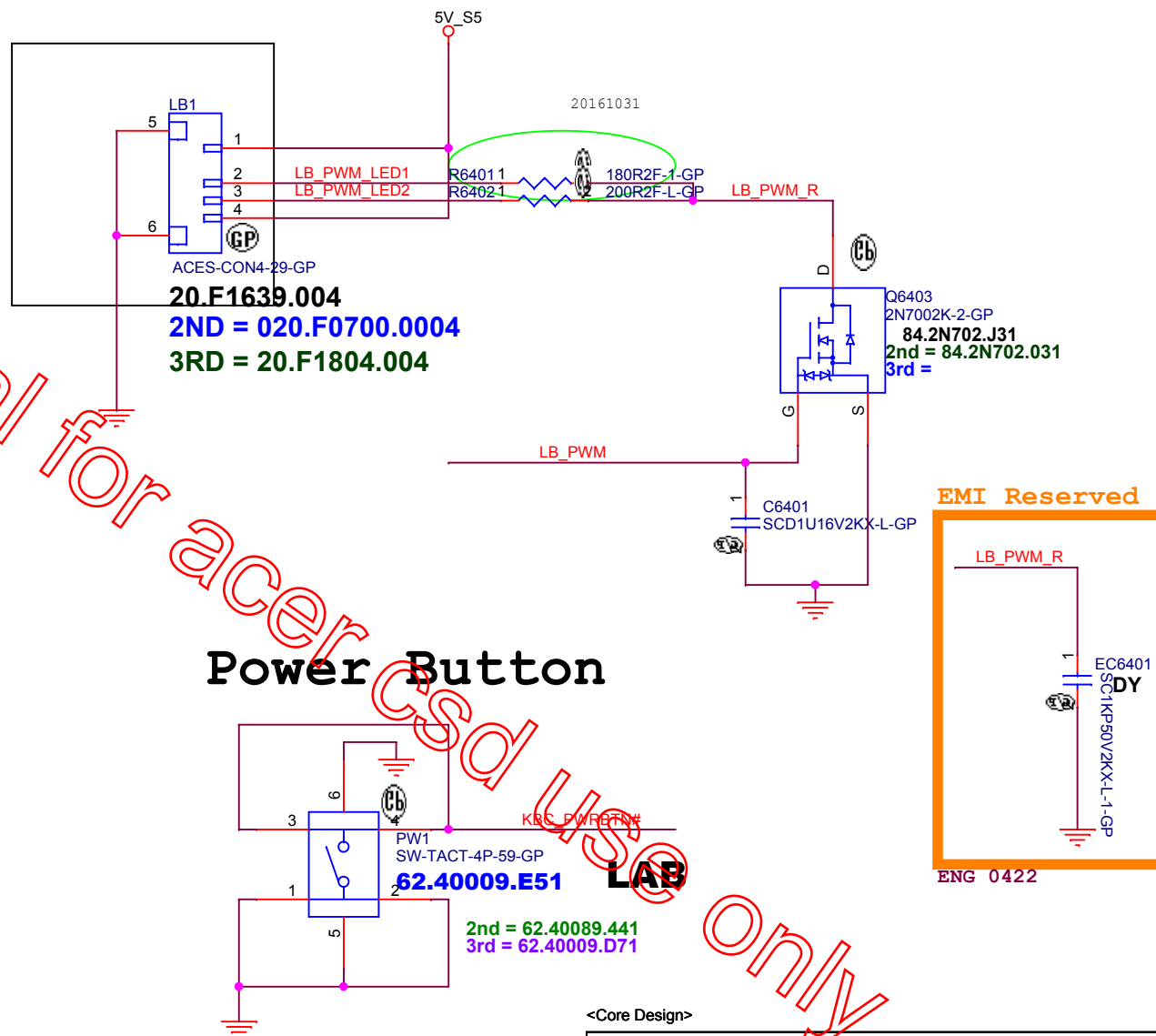
62.40009.E51

2nd = 62.40089.441

3rd = 62.40009.D71

LAB

<Core Design>

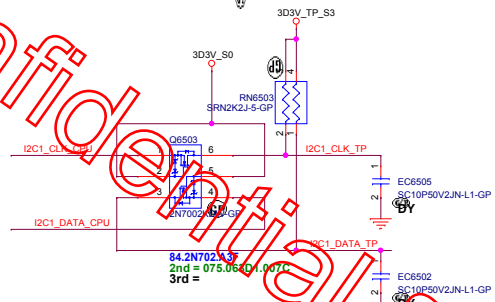
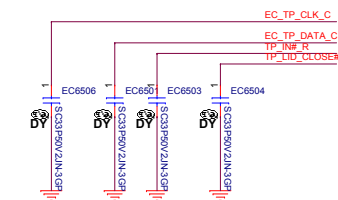
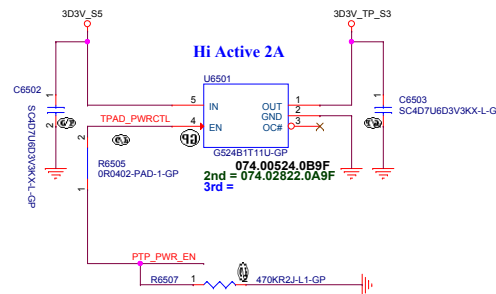
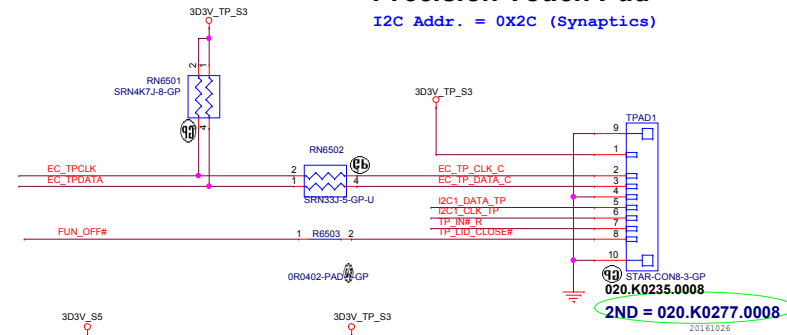
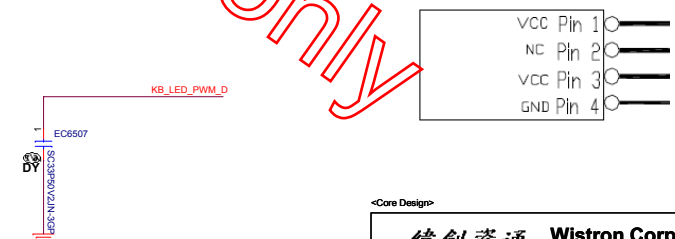
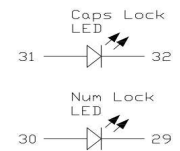
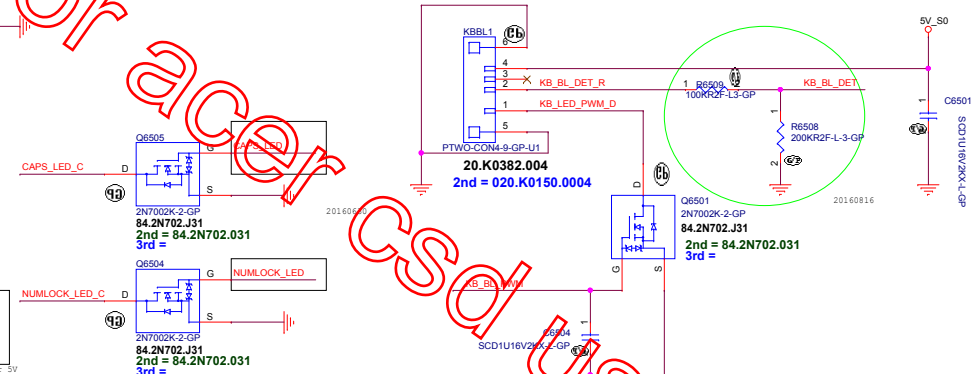


```

89 LB_PWM_LED1 >>> _____
89 LB_PWM_LED2 >>> _____

```

I2C Addr. = 0X2C (Synaptics)

[illegible]

Pin 1 location diagram showing the top side of the component. The diagram includes a legend for P1-VCC, PWR, and P2-GND. A table maps pin numbers to component pins. A note indicates that pins 1, 2, and 3 are not used.

Pin Number	Component Pin
32	Caps+
31	Num +
30	Num +
29	Num +
28	Num +
27	Num +
26	P1-VCC
25	R01
24	R02
23	R03
22	R04
21	R05
20	R06
19	R07
18	R08
17	R09
16	R10
15	R11
14	R12
13	R13
12	R14
11	R15
10	R16
9	R17
8	R18
7	C08
6	C07
5	C06
4	C05
3	C04
2	C03
1	C02

VIEW FROM TOP SIDE

PIN NUMBER

30

1, 2, 3 are not used

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Title			
LED Bard / Power Button			
Size	Document Number		Rev
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[illegible]

15,66 USB3_USB20_N
15,66 USB3_USB20_P

15 CARD1_USB20_N
15 CARD1_USB20_P

15,66 USB3_USB20_N
15,66 USB3_USB20_P

24,89 STDBY_LED
24,89 PWRLED
24,89 CHARGE_LED
24,89 DC_BATFULL

27,89 AUD_HP1_ID#
27,66,89 AUD_HP1_JACK_L2
27,66,89 AUD_HP1_JACK_R2

20160621 27,66 AUD_SPDIF_OUT
24,35 USB_PWR_EN
AFTP TESTPOINT

89 CARD1_USB20_CON_N
89 CARD1_USB20_CON_P
89 USB3_USB20_CON_N
89 USB3_USB20_CON_P
89 USB4_USB20_CON_N
89 USB4_USB20_CON_P

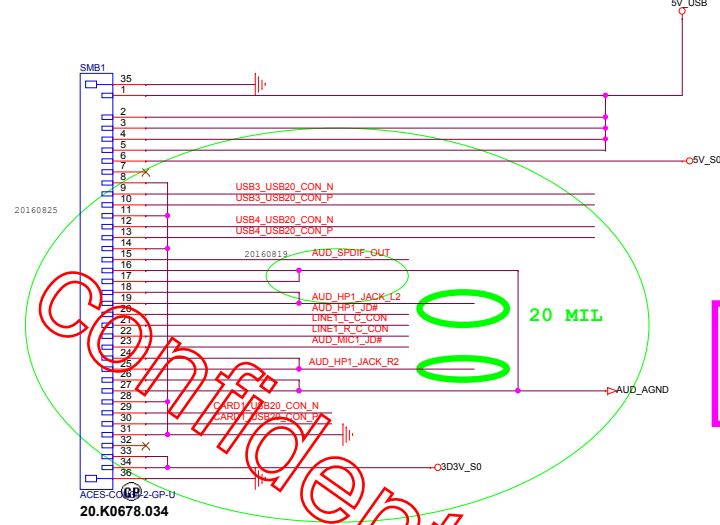
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24,89 LID_CLOSE#

27,66 AUD_MIC1_ID#

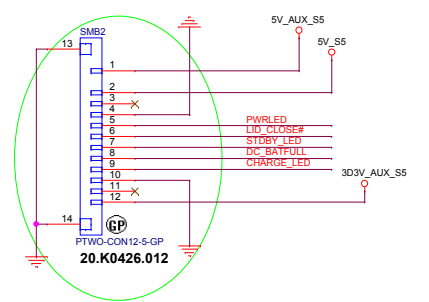
27 LINE1_VREF0_L
27 LINE1_VREF0_R

PLUTO
15 USB4_USB20_N
15 USB4_USB20_P
27,66 AUD_MIC1_ID#

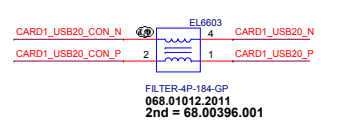
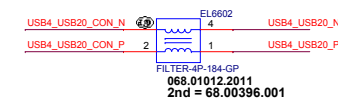
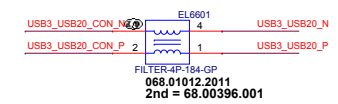
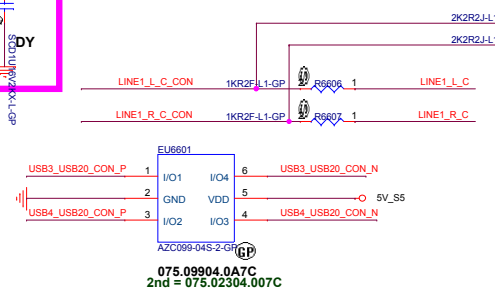
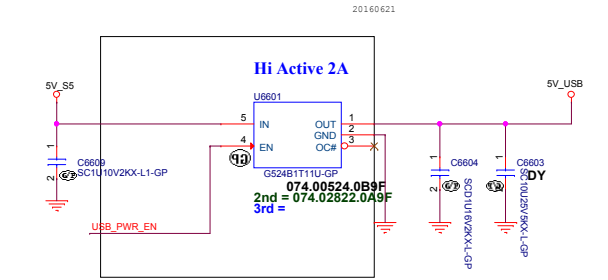
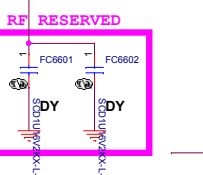
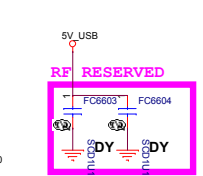
27 LINE1_L_C
27 LINE1_R_C



Neptune Daughter Board
USB2_0 *2
SPDIF*1
MIC*1
Card Reader *1



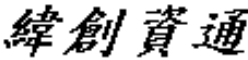
Neptune Daughter Board
LED(charger, standby, power dc full)
Hall Sensor

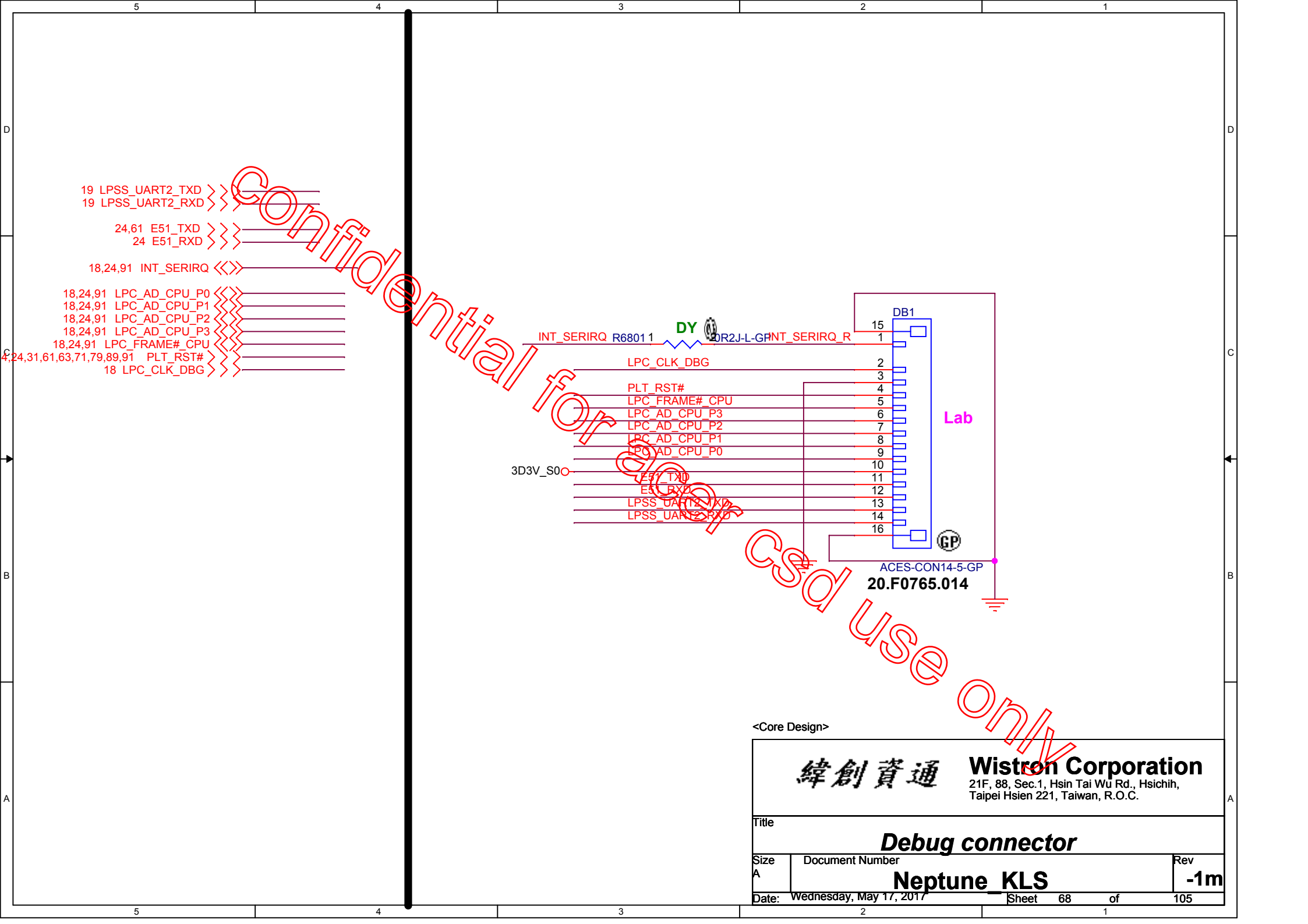


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IO Board Connector			
Neptune_KLS			
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Custom		-1m	
Date	Wednesday, May 17, 2017	Sheet	66 of 105

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Title			
Hall Sensor			
Size A	Document Number		Rev
	Neptune_KLS		-1m
Date:	Wednesday, May 17, 2017		Sheet 67 of 105



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Title

Debug connector

Size

Document Number

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Neptune KLS

-1m

Date:

Wednesday, May 17, 2017

Sheet

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of

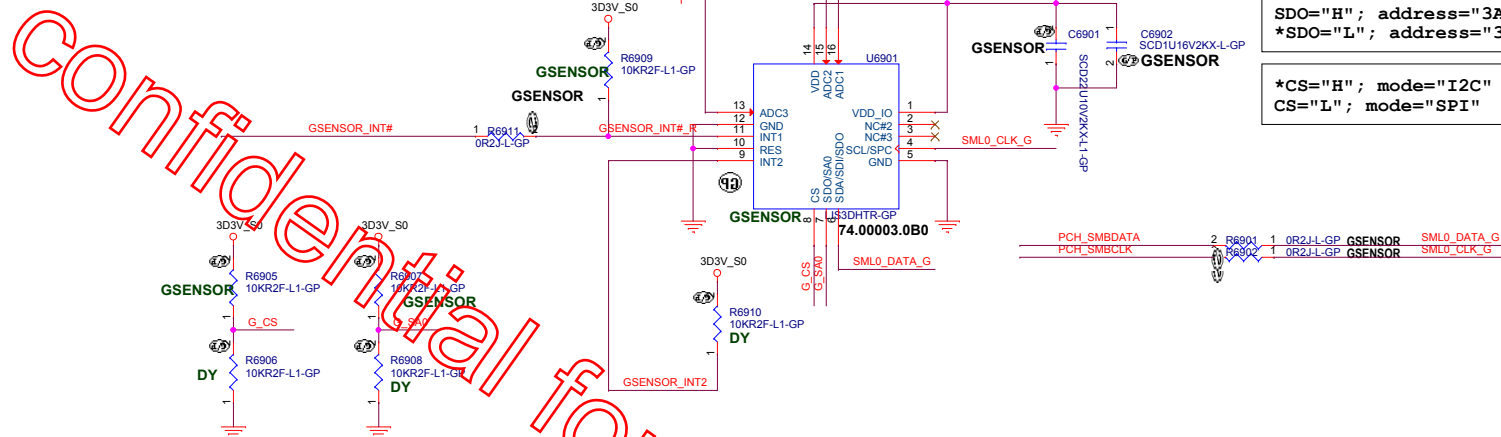
105

SSID = User.Interface

G Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



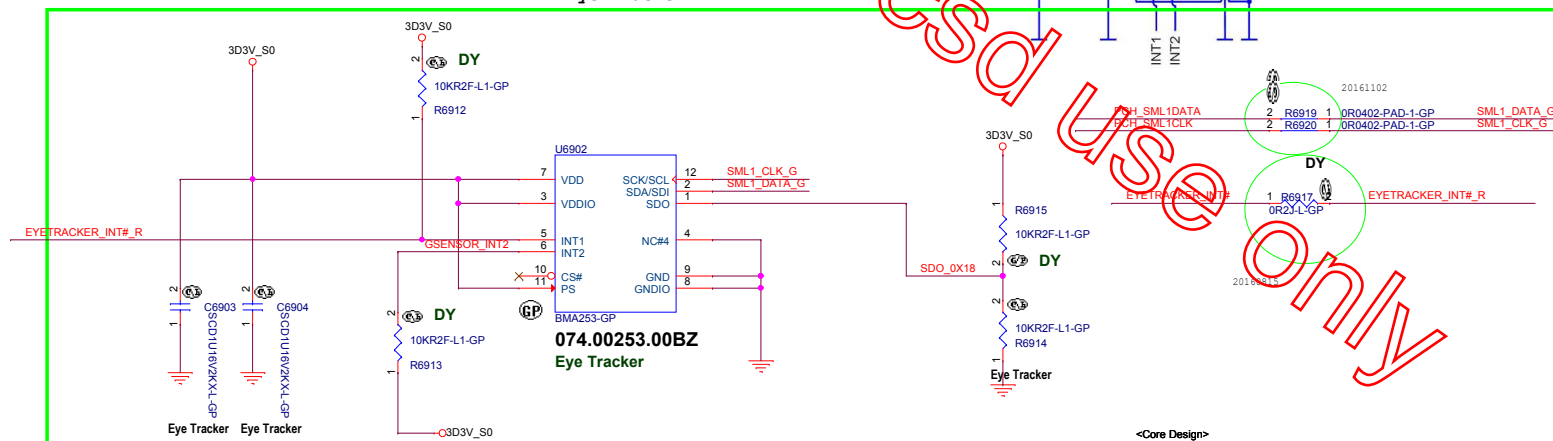
SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

SSID = User.Interface

G Sensor (BMA253 I2C address 0x18)

Eye Tracker



The default I2C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'VDDIO'.

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title G-SENSOR

Size Document Number

Custom Neptune KLS

Date: Wednesday, May 17, 2017

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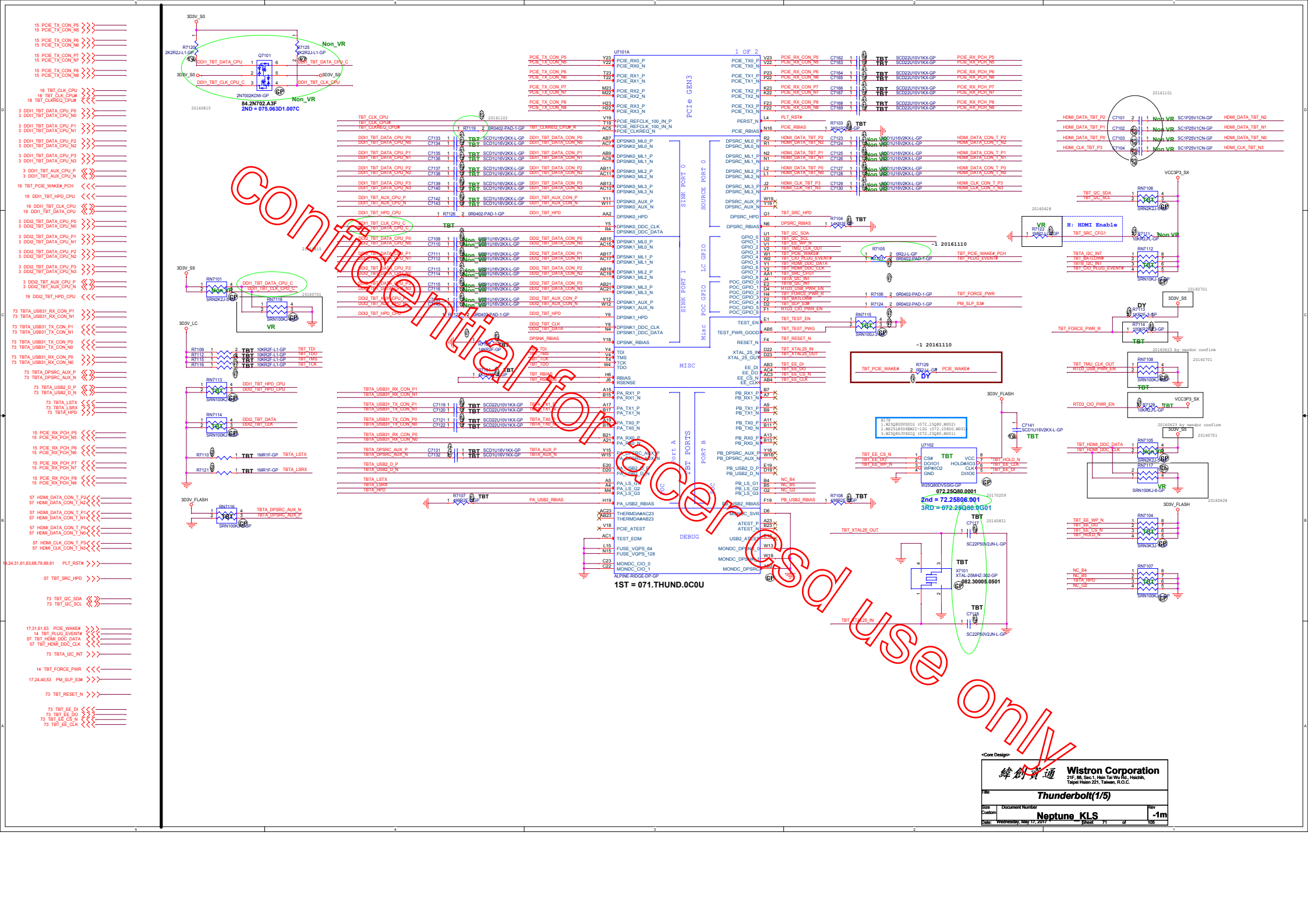
105

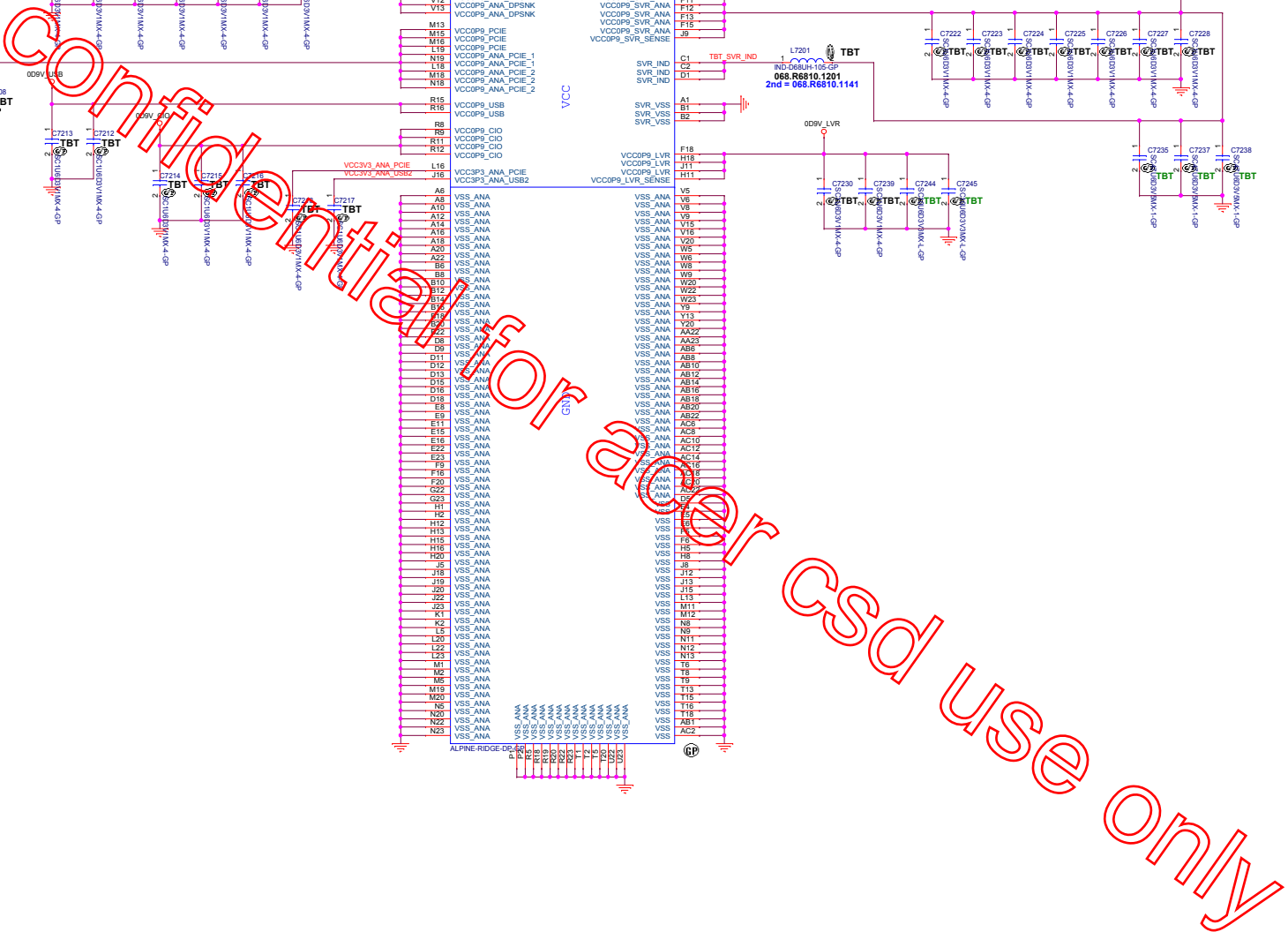
Rev -1m

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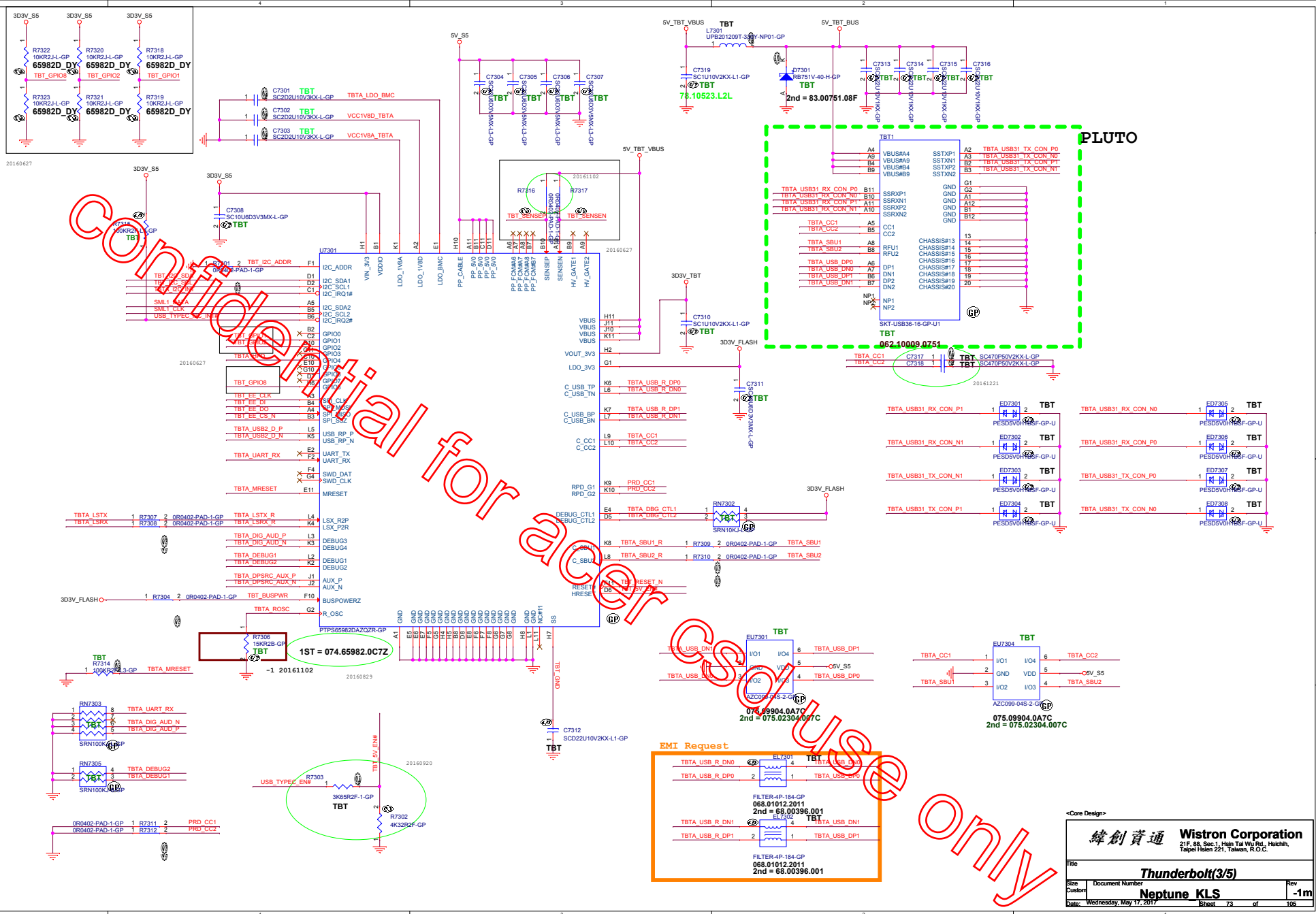
<Core Design>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)Free Fall Sensor			
Size A	Document Number Neptune_KLS		Rev -1m
Date: Wednesday, May 17, 2017		Sheet 70 of	105





71 TBT_RESET_N <<<
71 TBT_I2C_SDA <<<
71 TBT_I2C_SCL <<<
71 TBT_I2C_INT <<<
17.24.79 SML1_DATA <<<
17.24.79 SML1_CLK <<<
24 USB_TYPEC_QC_INT# <<<
71 TBT1_HPD <<<
71 TBT_EE_CLK <<<
71 TBT_EE_DI <<<
71 TBT_EE_DO <<<
71 TBT_EE_CS_N <<<
71 TBT1_USB2_D_P <<<
71 TBT1_USB2_D_N <<<
24 TBT1_MRESET >>>
71 TBT1_LSTX <<<
71 TBT1_LSRX <<<
24 USB_TYPEC_EN# >>>
71 TBT1_DPSRC_AUX_P <<<
71 TBT1_DPSRC_AUX_N <<<
24 USB_TYPEC_EN# >>>
71 TBT1_USB31_TX_CON_P0 <<<
71 TBT1_USB31_TX_CON_N0 <<<
71 TBT1_USB31_TX_CON_P1 <<<
71 TBT1_USB31_TX_CON_N1 <<<
71 TBT1_USB31_RX_CON_P0 <<<
71 TBT1_USB31_RX_CON_N0 <<<
71 TBT1_USB31_RX_CON_P1 <<<
71 TBT1_USB31_RX_CON_N1 <<<



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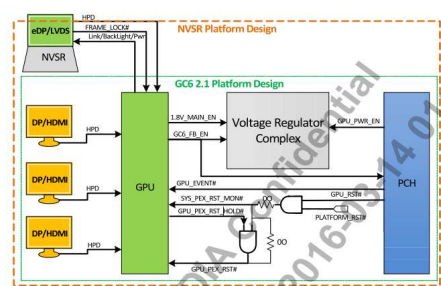
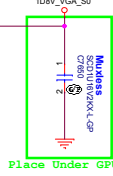
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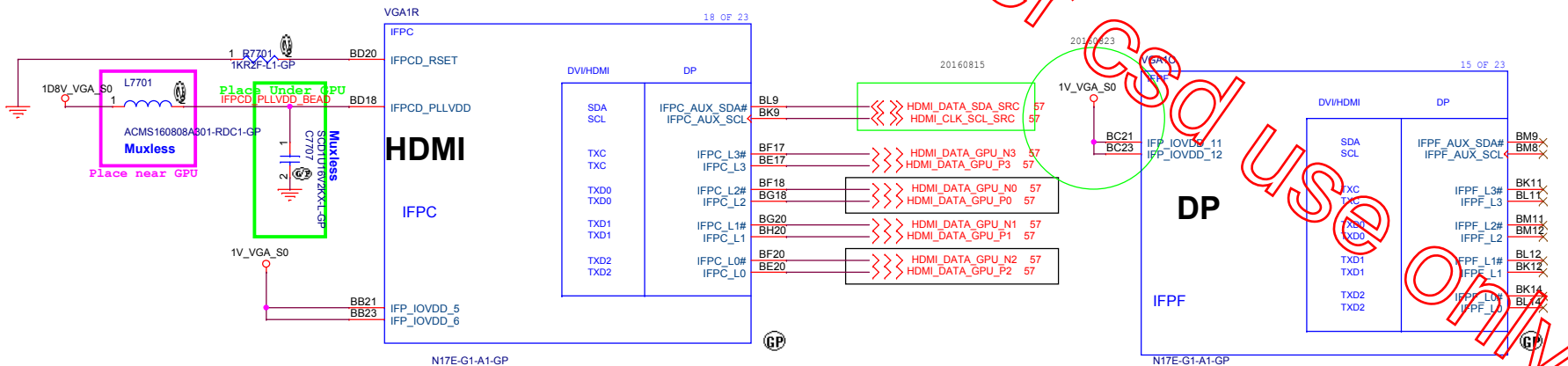
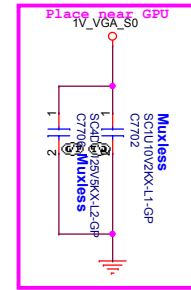
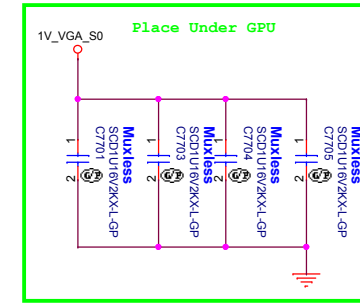
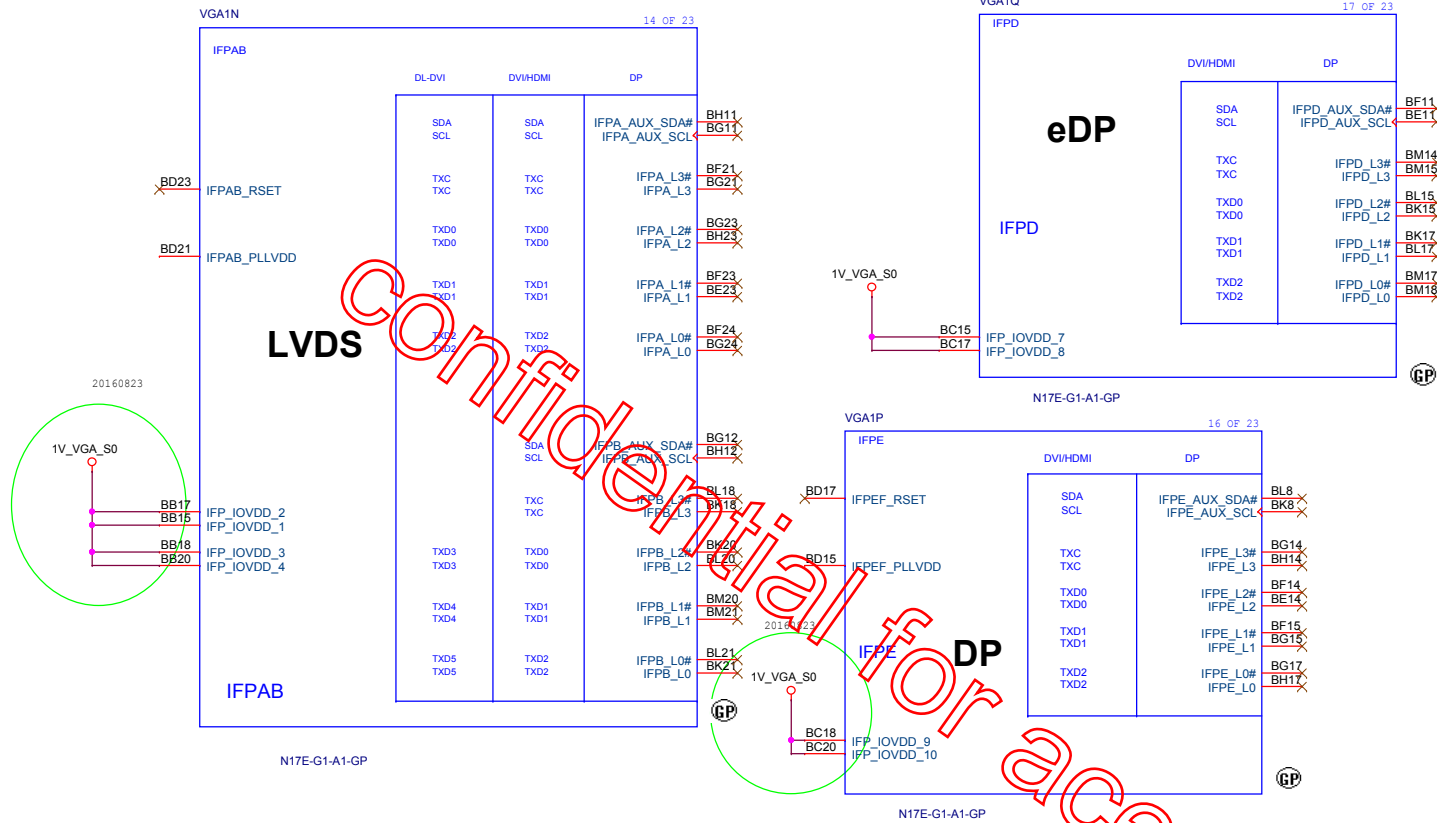
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)Thunderbolt (4/5)			
Size A	Document Number Neptune_KLS		Rev -1m
Date: Wednesday, May 17, 2017		Sheet 74 of	105

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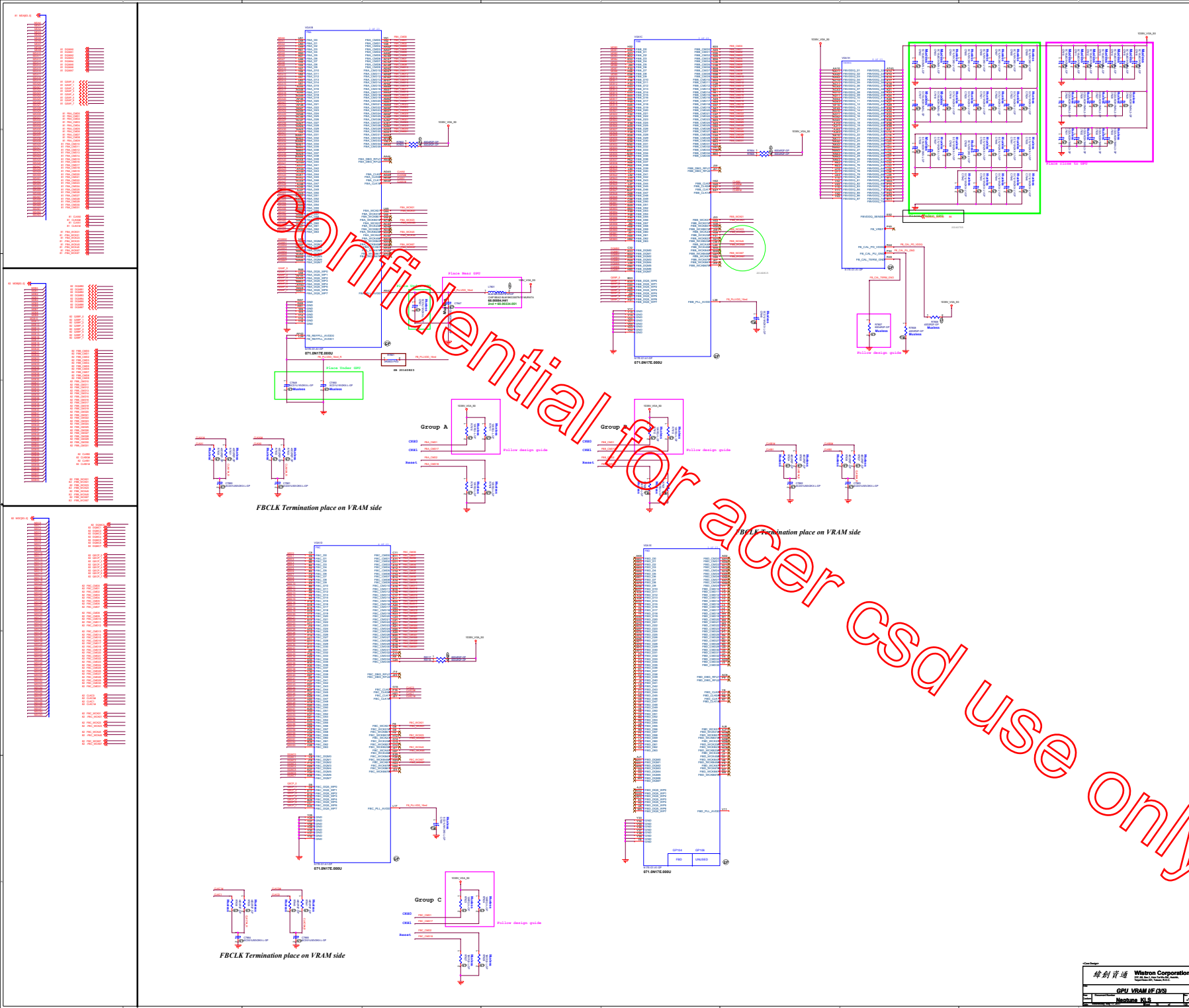
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>(Reserved)Thunderbolt (5/5)</div>		
Size <div>A</div>	Document Number <div>Neptune_KLS</div>	Rev <div>-1m</div>
Date: Wednesday, May 17, 2017		
Sheet 75 of 105		

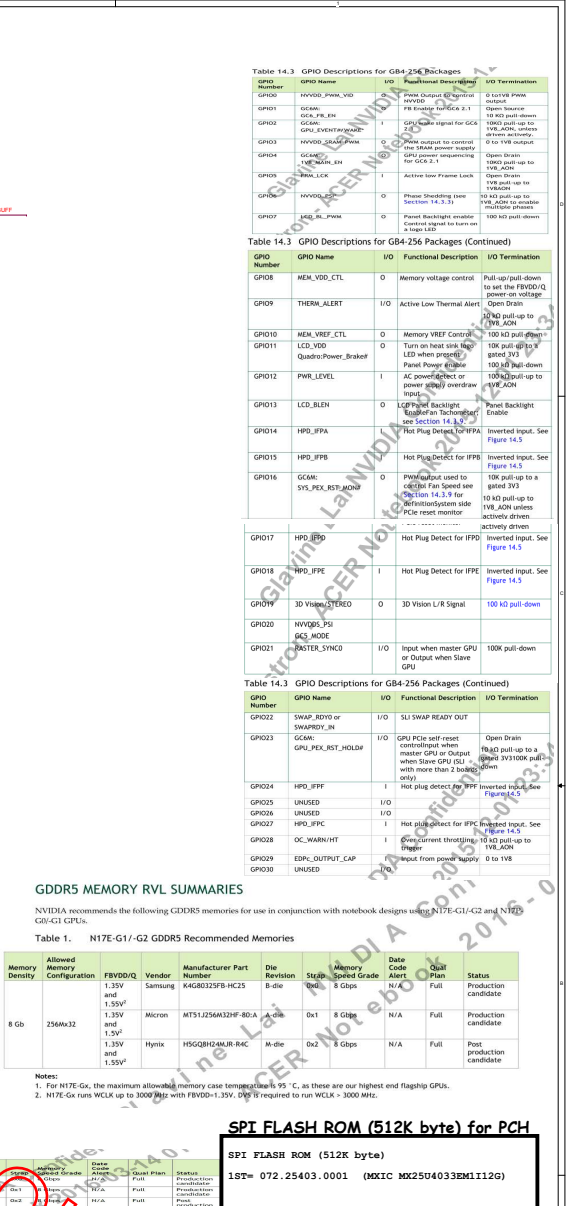
PEX_TEMP



<Core Design>



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GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO2	SWAP_RDY0 or SWAP_RDY1	I/O	SWI Swap READY OUT	
GPIO3	GCAR_GPIO_PEX_RST_HOLD0	I/O	GPIO PC self-reset controller when master GPIO or Output Enable Slave GPIO with more than 2 loaded outputs	Open Drain Pull-up to 10k 10V/100k pull
GPIO4	HFD_0FF0	I	Hot plug detect for IFC	Inverted, Input See Figure L2.5
GPIO5	UNLNRD	I/O		
GPIO6	UNLNRD	I/O		
GPIO27	HFD_0FF1	I	Hot plug detect for IFC	Inverted, Input See Figure L2.5
GPIO8	OC_WARNH0T	I	Over current threshold	10k pull-up to 10V, J40H
GPIO9	ESDP_OUTPUT_CAP_UNLNRD	I/O	Input from power supply	0 to 1VS
GPIO10	UNLNRD	I/O		

NVIDIA recommends the following GDDR5 memories for use in conjunction with notebook designs using N17E-G1/G2 and N17P-G0/G1 GPUs.

Altitude									Date	of	
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Notes:

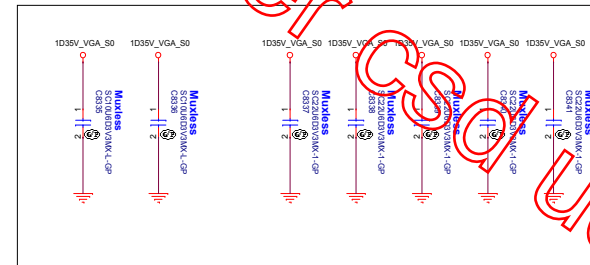
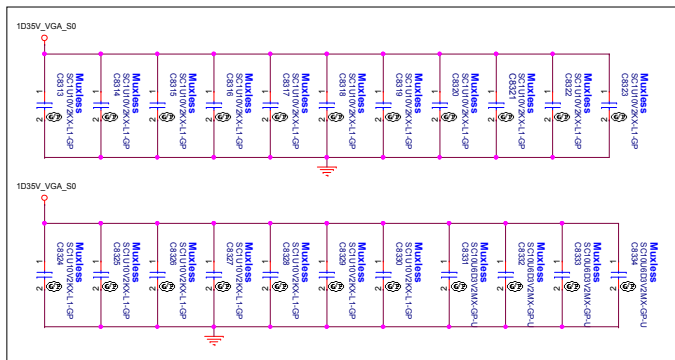
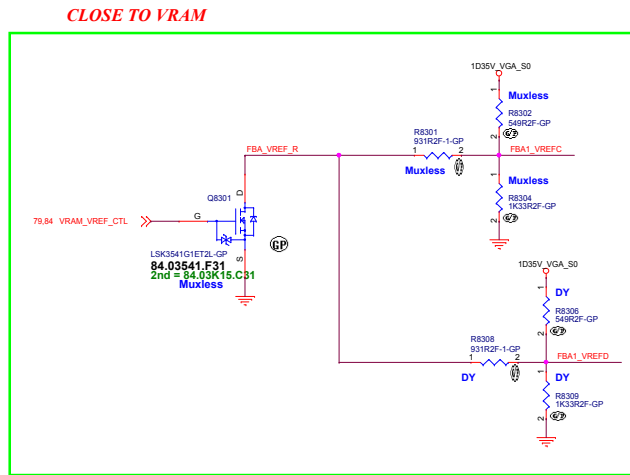
1. For N17E-Gx, the maximum allowable memory case temperature is 95 °C, as these are our highest end flagship GPUs.
2. N17E-Gx runs WCLK up to 3000 MHz with FBVDD=1.35V. DVS is required to run WCLK > 3000 MHz.

SPI FLASH ROM (512K byte)

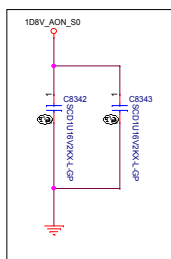
Strap Pins <small>see Note</small>			RAMCFG Setting Number
STRAP2*	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

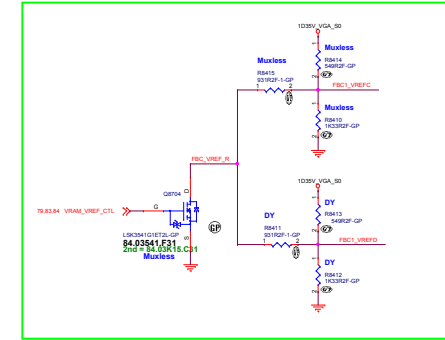
Core Design		Wistron Corporation	
緯創資通		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei 30521, Taiwan, R.O.C.	
File			
GPU GPIO/STRAP			
Size	Document Number		Rev
N1	Neptune	KLS	-1
Date:	Wednesday, May 17, 2017	Sheet	78 of 105



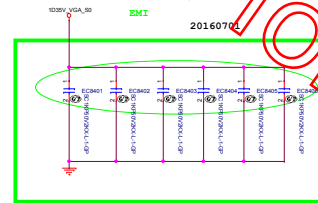


CLOSE TO THE MEMORY

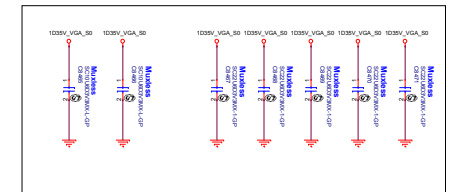




CLOSE TO VRAM

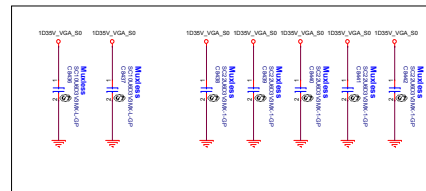


CLOSE TO THE MEMORY

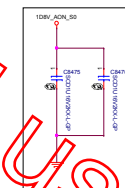


CLOSE TO THE MEMORY

UNDER TO THE MEMOR



UNDER THE MEMORY



UNDER THE MEMORY

VGA : N17E-G1
Config : B
EDP-Continuous : 58A
EDP-Peak : 136A

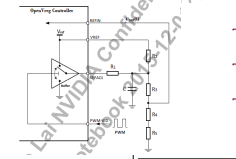
CHECK SPEC

1. VCC_VGA_P1
2. VCC_VGA_P2
3. VCC_VGA_P3
4. VCC_VGA_P4
5. VCC_VGA_P5
6. VCC_VGA_P6
7. VCC_VGA_P7
8. VCC_VGA_P8
9. VCC_VGA_P9
10. VCC_VGA_P10
11. VCC_VGA_P11
12. VCC_VGA_P12
13. VCC_VGA_P13
14. VCC_VGA_P14
15. VCC_VGA_P15
16. VCC_VGA_P16
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92. VCC_VGA_P92
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95. VCC_VGA_P95
96. VCC_VGA_P96
97. VCC_VGA_P97
98. VCC_VGA_P98
99. VCC_VGA_P99
100. VCC_VGA_P100

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4. VCC_VGA_P4
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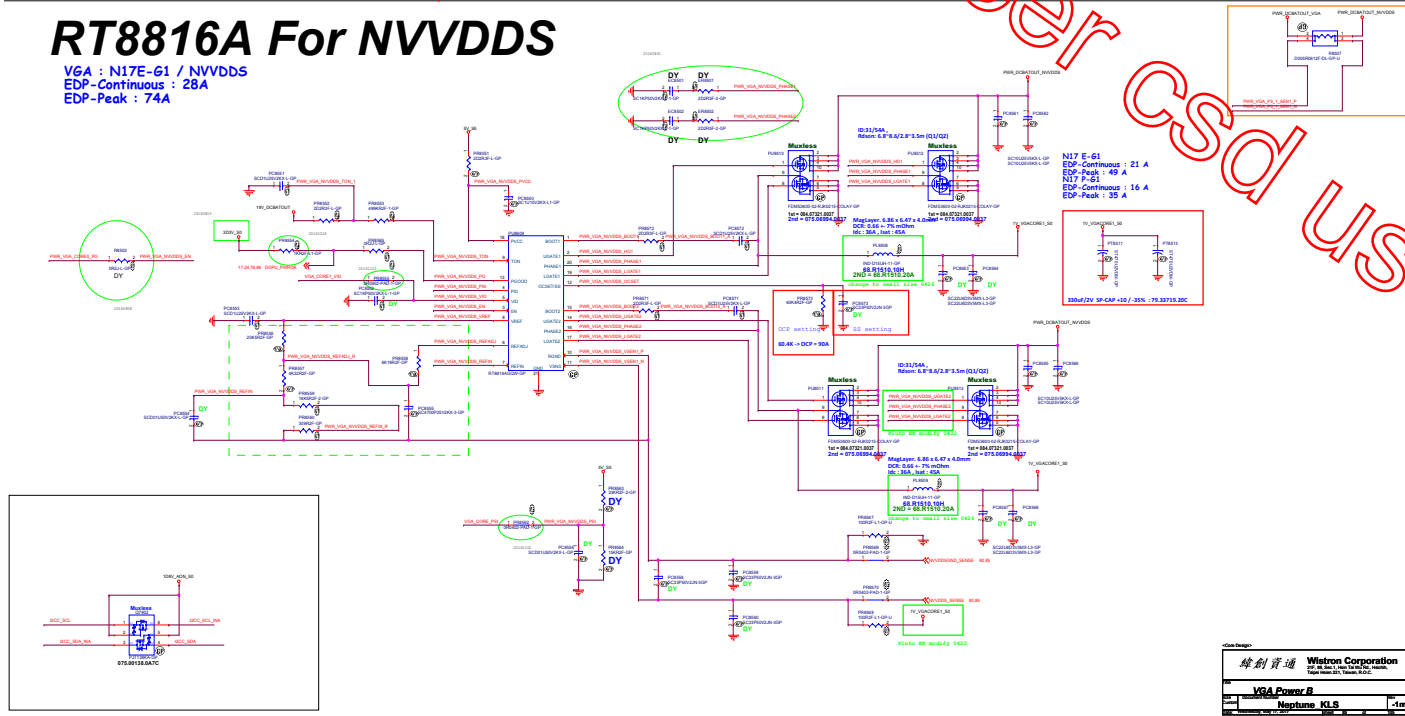
Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification			
	Unit	Config	
Number of Voltage Levels H	level	160	
PWM Frequency F _{sw}	kHz	675	
PWM Minimum Pulse Width T _{min}	ns	9.26	
VID Transient Time T _{tr}	ns	<100	
Component Value			
R1 (1%)	Ω	6.19	
R2 (1%)	Ω	20.5	
R3 (1%)	Ω	4.32	
R4 (1%)	Ω	14.5	
R5 (1%)	Ω	6.29	
C	μF		

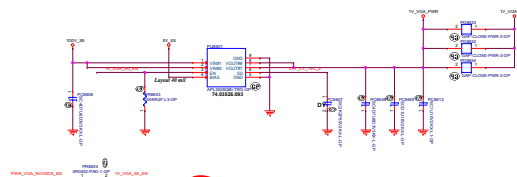


RT8816A For NVVDDS

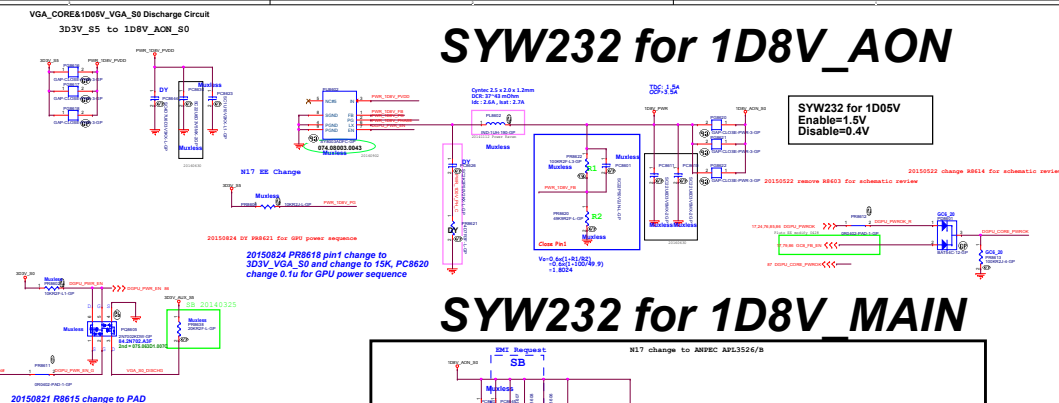
VGA : N17E-G1 / NVVDDS
EDP-Continuous : 28A
EDP-Peak : 74A



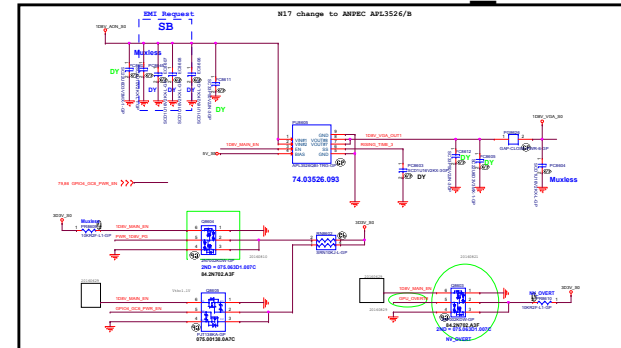
APL3526QB for 1V_VGA_S0



SYW232 for 1D8V_AON



SYW232 for 1D8V_MAIN



RT8816A for PWR_VGA_CDDR

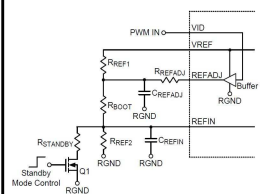


Figure 9. PWM VID Analog Circuit Diagram

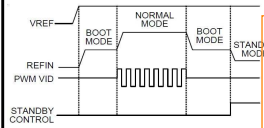
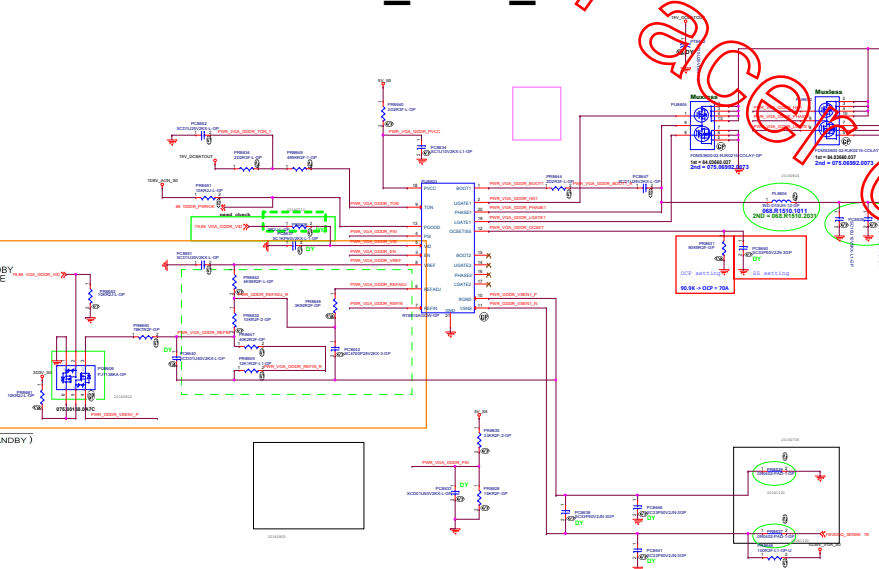


Figure 10. PWM VID Time Diagram

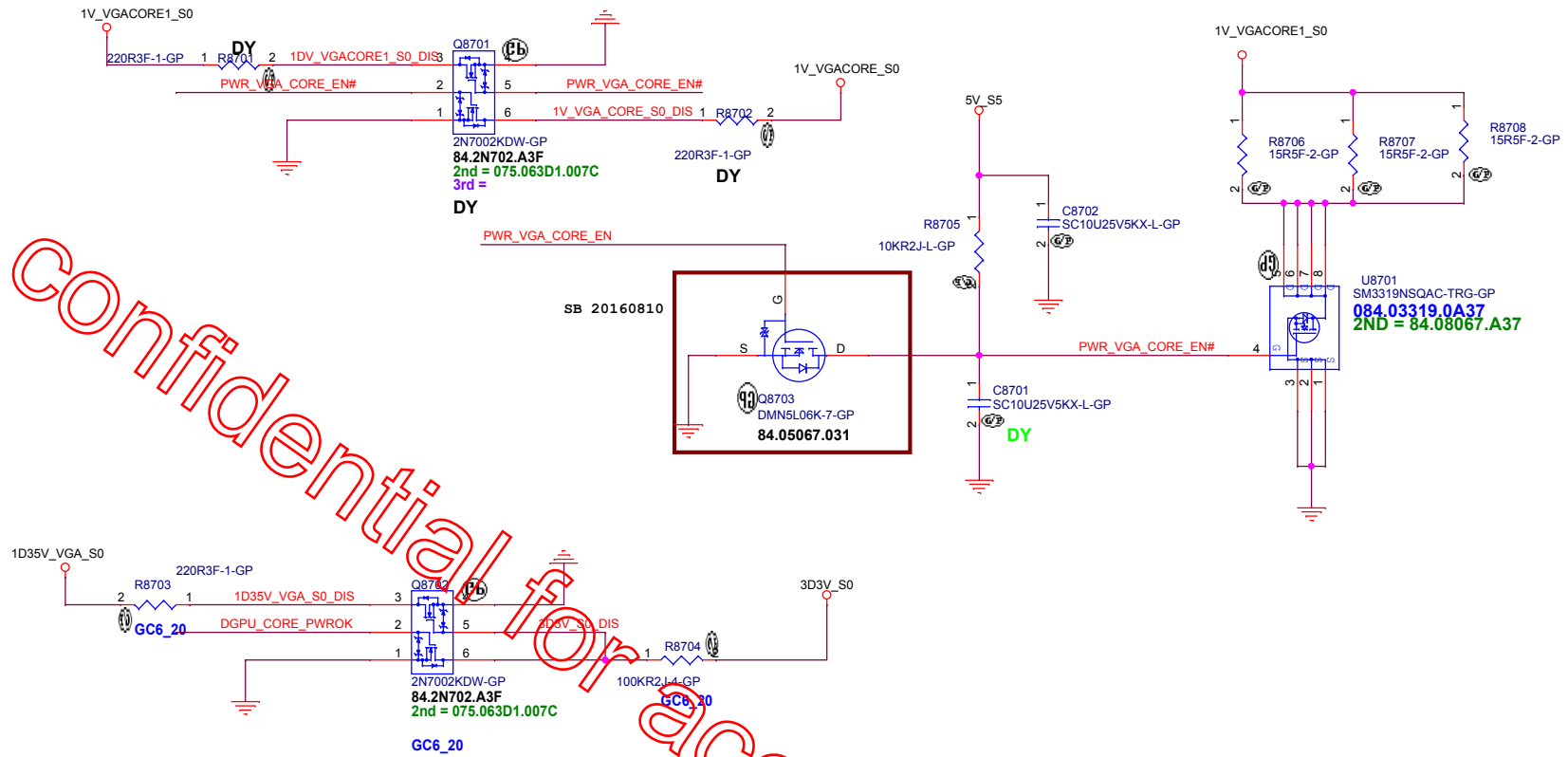
$$V_{BOOT} = V_{REF} \times \left(\frac{R_{REF2}}{R_{REF1} + R_{REF2} + R_{BOOT}} \right)$$

$$V_{STANDBY} = V_{REF} \times \left(\frac{R_{REF2} // R_{STANDBY}}{R_{REF1} + R_{BOOT} + (R_{REF2} // R_{STANDBY})} \right)$$



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85 PWR_VGA_CORE_EN
86 DGPU_CORE_PWROK

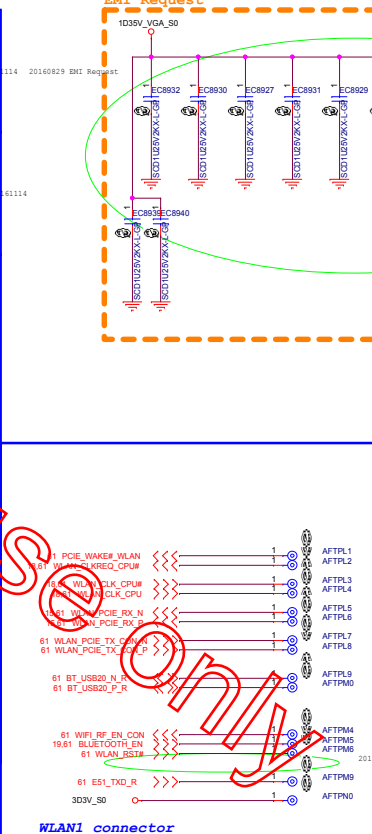
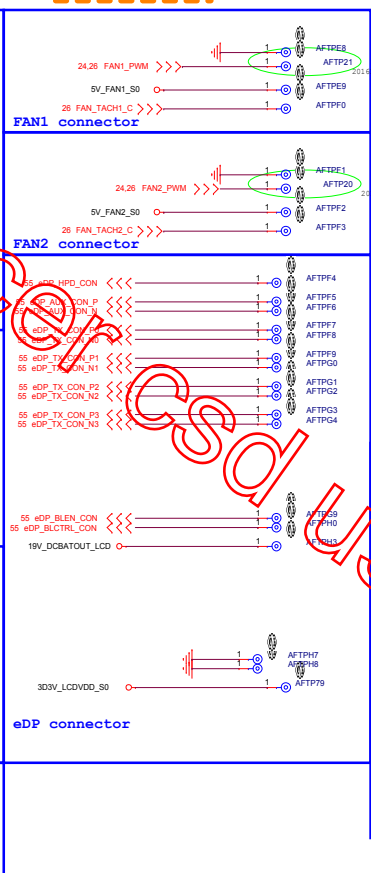
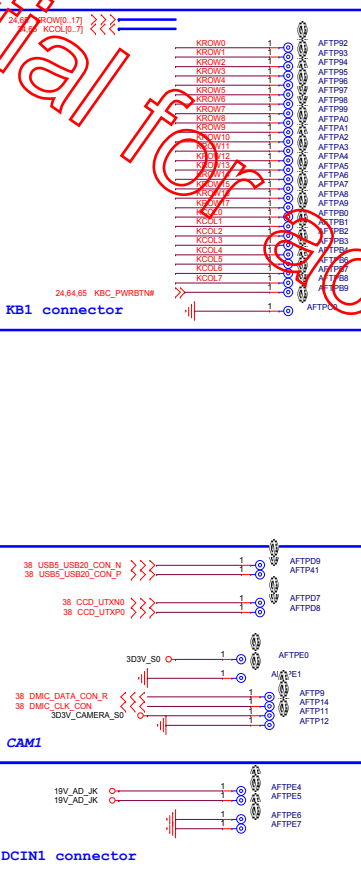
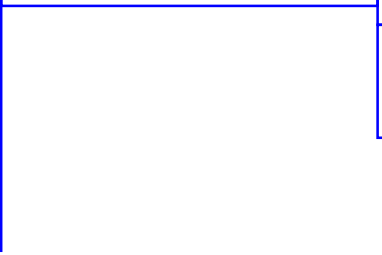
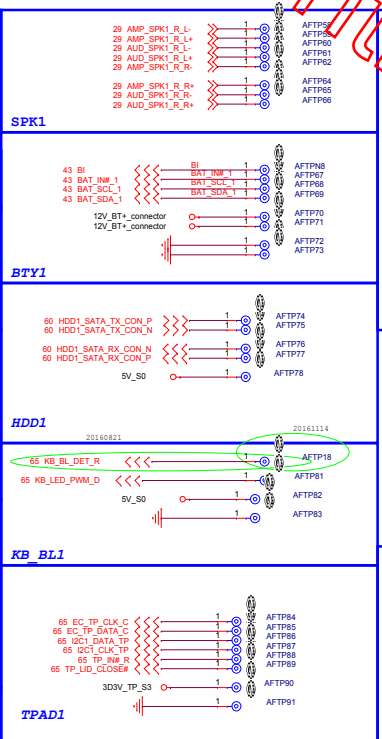
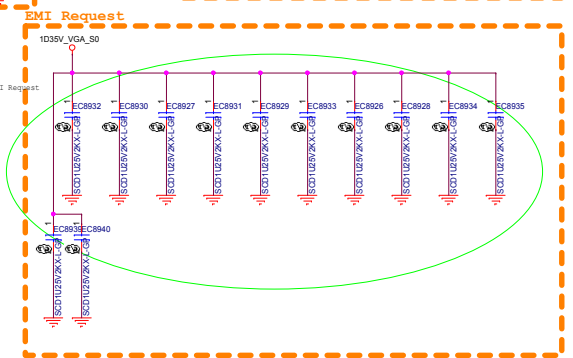
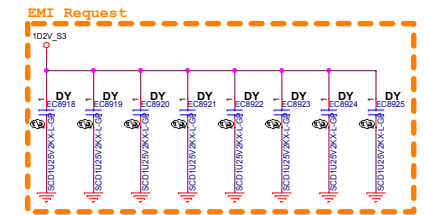
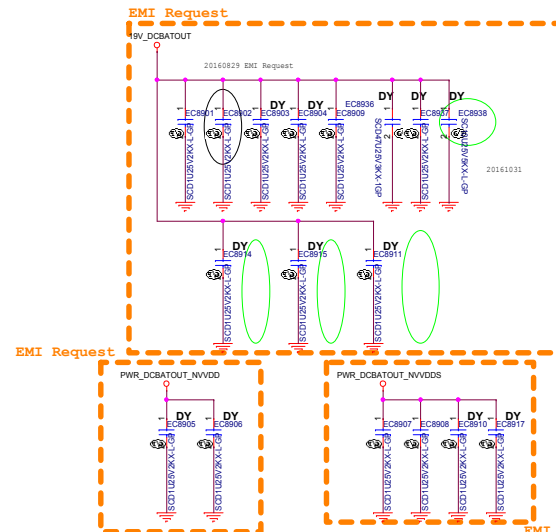


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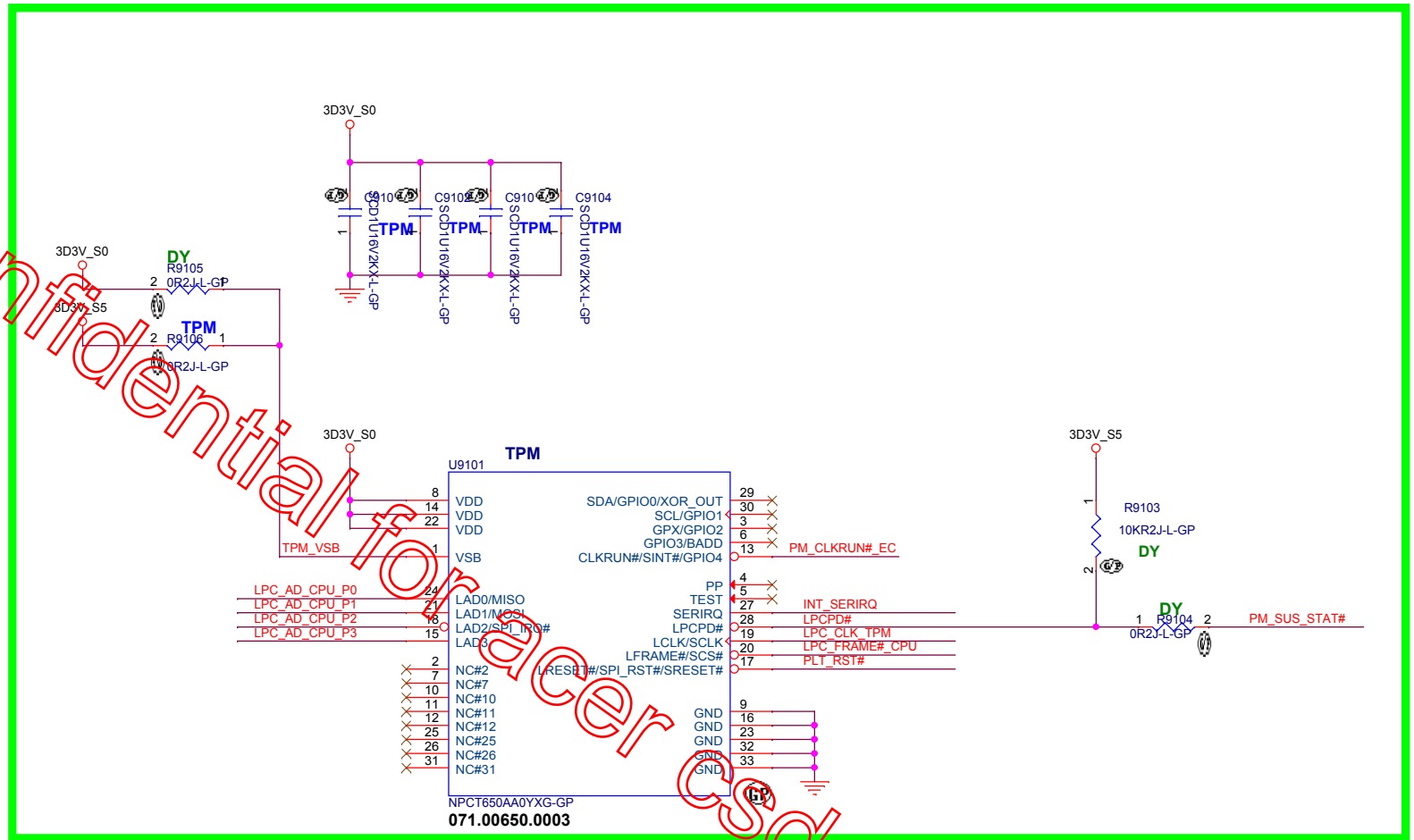
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PLUTO

18,24,68 LPC_FRAME#_CPU <<<
 18,24,68 INT_SERIRQ <<<
 18 PM_SUS_STAT# <<<
 18 LPC_CLK_TPM <<<
 14,24,31,61,63,68,71,79,89 PLT_RST# <<<
 17,24 PM_CLKRUN#_EC <<<

18,24,68 LPC_AD_CPU_P0 <<<
 18,24,68 LPC_AD_CPU_P1 <<<
 18,24,68 LPC_AD_CPU_P2 <<<
 18,24,68 LPC_AD_CPU_P3 <<<



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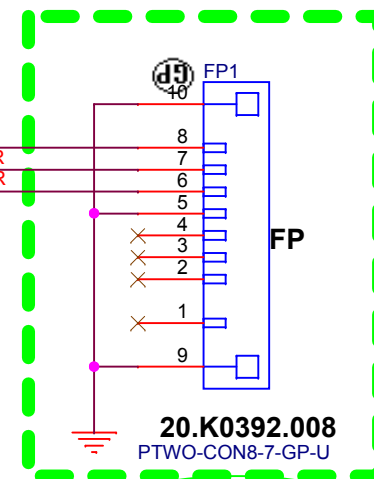
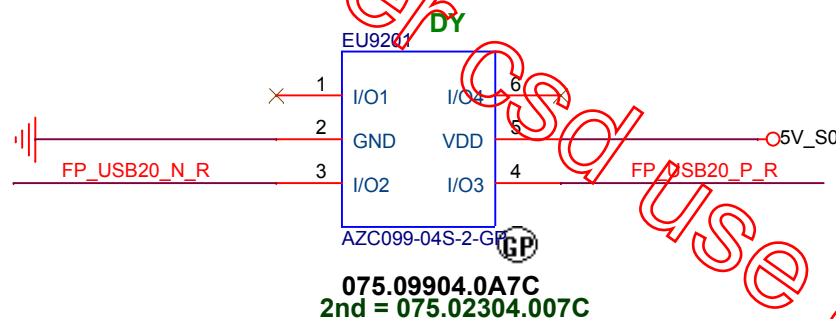
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15 FP_USB20_P
15 FP_USB20_N

5V_S0
FP_USB20_P 2 ER9201 1 0R0402-PAD-1-GP FP_USB20_P_R
FP_USB20_N 2 ER9202 1 0R0402-PAD-1-GP FP_USB20_N_R

C9201
10V2KX-L1-GP

FP



20170210

20160701

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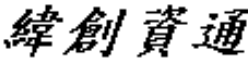
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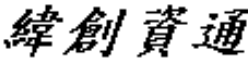
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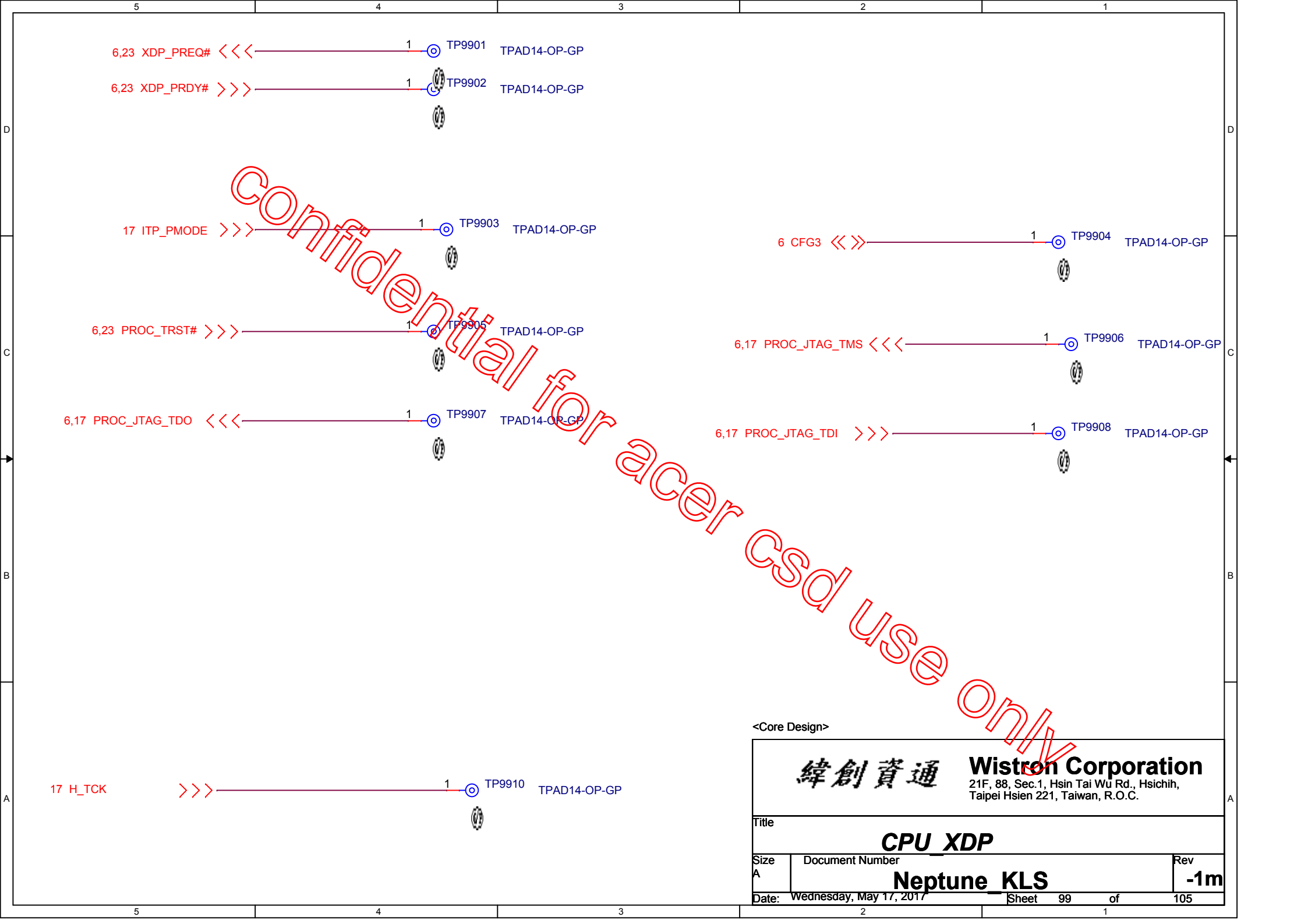
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CPU CFG CFG STRAP			
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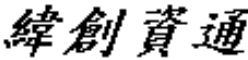
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The diagram illustrates the timing relationships for various power and control signals during the transition from AC mode to DC mode. The signals are organized into two main sections: AC mode (DC mode) and DC mode.

AC mode (DC mode) signals:

- RTC_AUX_S5
- RTC_RST#
- 3D3V_AUX/SV_AUX
- EOREST
- SV_CHARGER_EN
- 3V_SV_EN
- SV_S5/3D3V_S5
- 3V_SV_POK
- DSMRST#
- AC_PRESENT
- KBC_PWRBTN_ECH
- 3V_SV_POK
- PM_PWRBTN#

DC mode signals:

- PM_SLP_S4#
- PM_PWRBTN#
- ZDSV_S3(VPP)
- VCCST
- VCCSTG
- 1D2V_S3(VDDQ)
- PM_SLP_S3#
- 0D4V_S0(VTT)
- SV_S0
- 3D3V_S0
- 1D8V_S0
- 99ms
- ALL_SYS_PWRGD
- VCCST_PWRGD
- PCH_PWRGD
- SYS_PWRGD
- PLT_RST#
- VCC
- VCCGT

Discrete only signals:

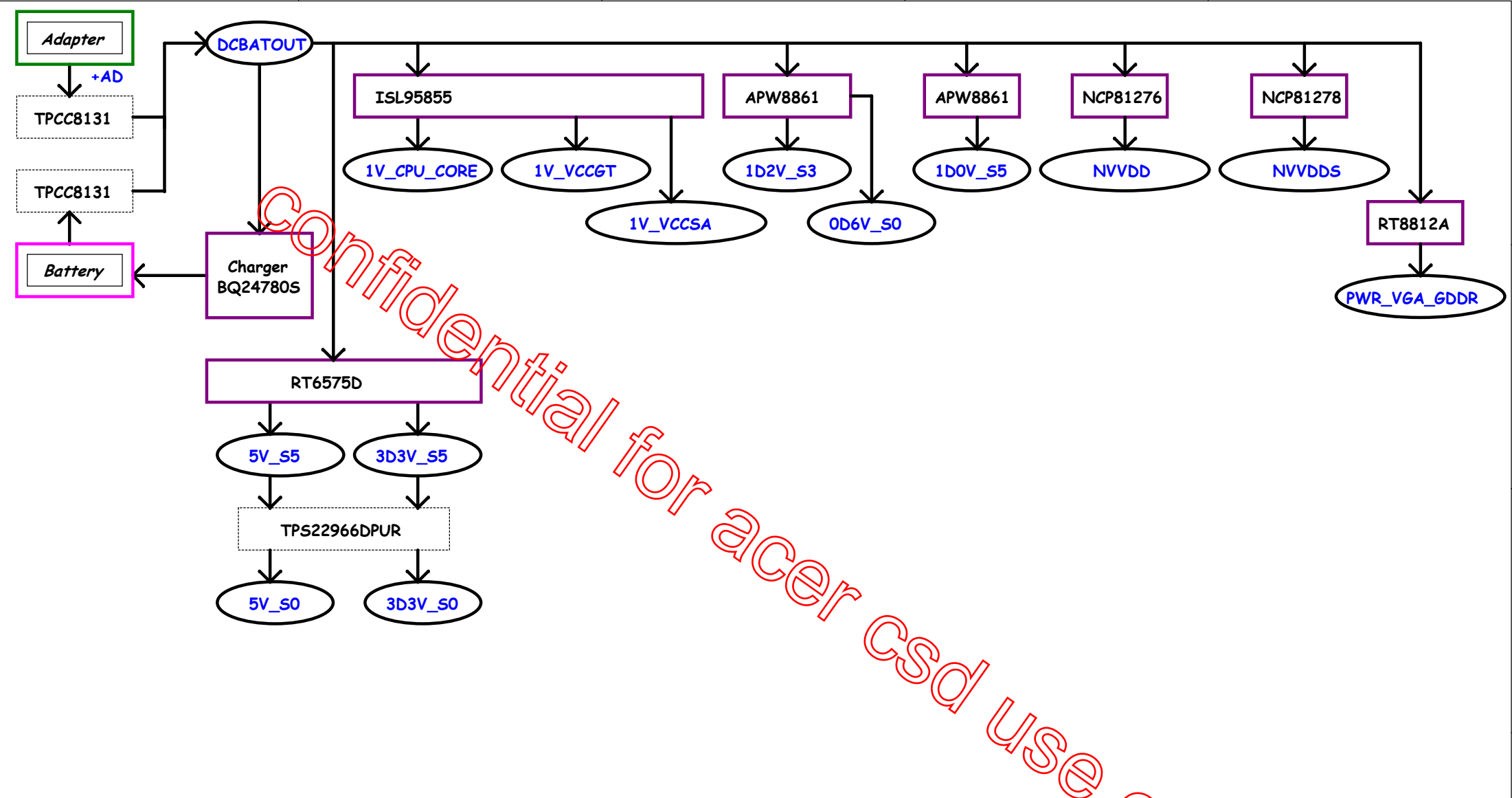
- DGPU_PWR_EN#
- 3D3V_VGA_S0
- VGA_CORE
- DGPU_PWRGD
- 1D8V_VGA_S0

DC mode signals (continued):

- 1D8V_S0_PWRGD
- ALL_SYSTEM_PWRGD
- CLK_CPU_BCLK
- CLKIN_BCLK Stable
- IMVP_PWRGD
- PCH_PWRGD
- PROC_PWRGD
- SYS_PWRGD
- ALL_SYSTEM_PWRGD
- PLT_RST#
- VCC_CORE

Annotations:

- To KBC GPST delay 99ms to PCH
- CPU CORE Power



Regulator

LDO

Switch

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Power Block Diagram

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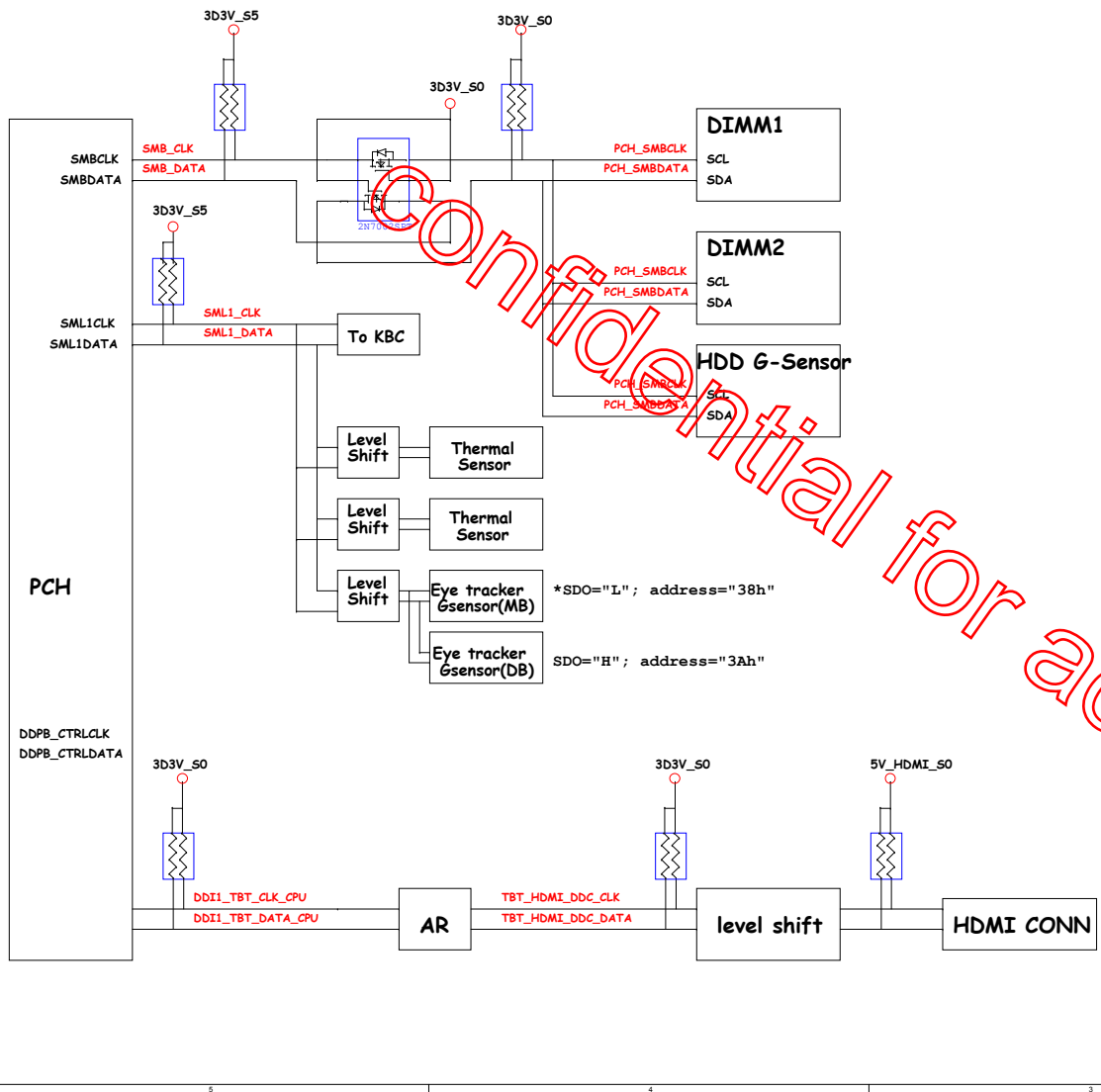
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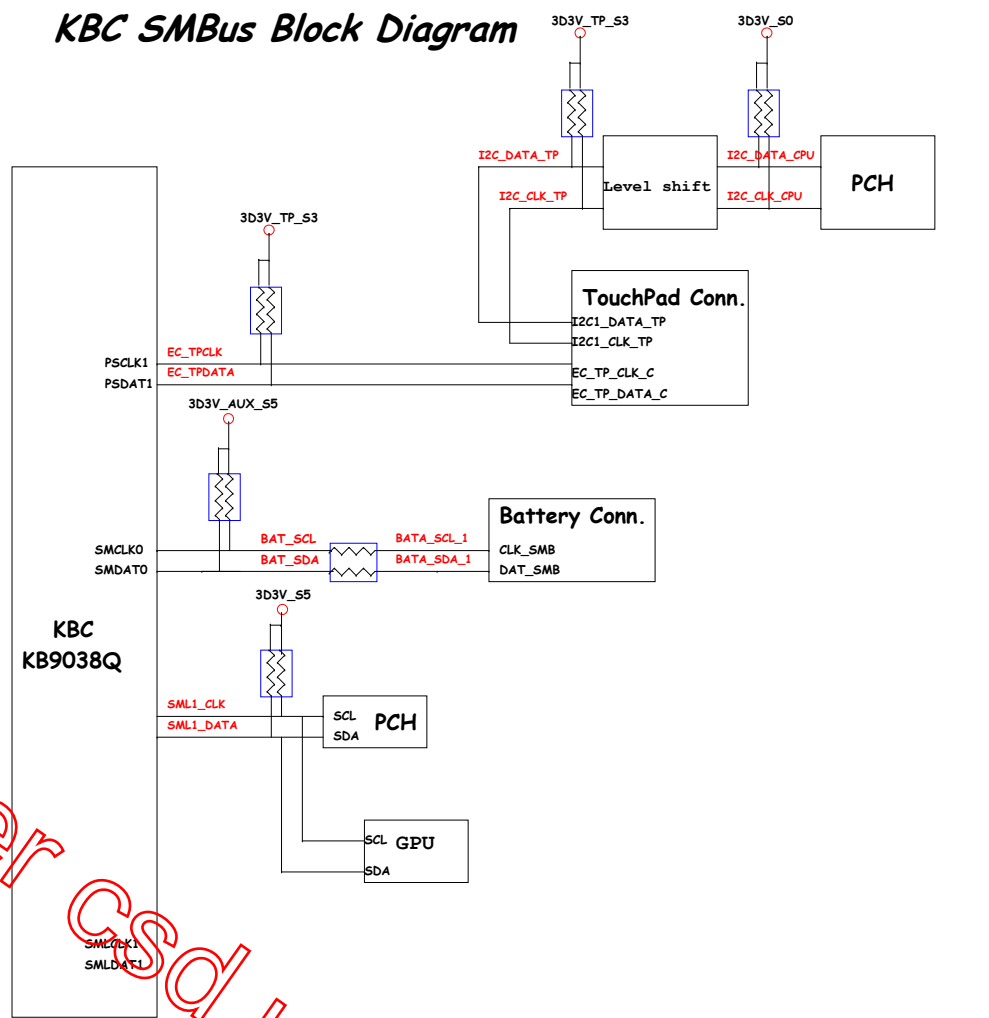
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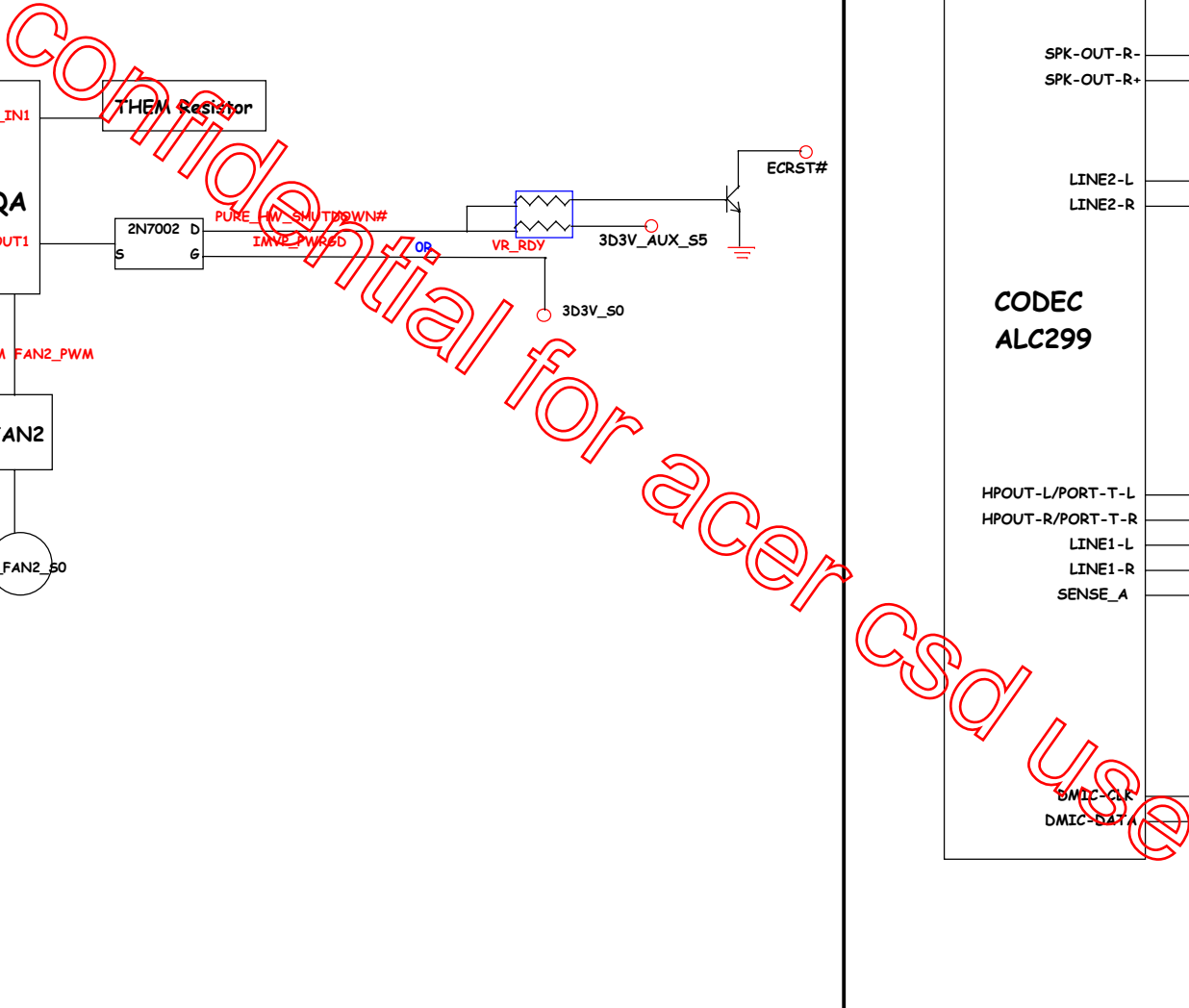
PCH SMBus Block Diagram



KBC SMBus Block Diagram



The schematic diagram illustrates the ALC299 CODEC's connections to the CPU and various components. The CPU side includes pins IN1, OUT1, FAN2_PWM, and FAN2_S0. The ALC299 CODEC has pins SPK-OUT-R-, SPK-OUT-R+, LINE2-L, LINE2-R, HPOUT-L/PORT-T-L, HPOUT-R/PORT-T-R, LINE1-L, LINE1-R, SENSE_A, SMDL-CLK, and DMIC-DATA. The diagram shows a THERM Resistor connected to IN1 and a 2N7002 MOSFET connected to OUT1. The MOSFET's gate is connected to IN1, and its drain is connected to FAN2_PWM. The MOSFET's source is connected to FAN2_S0. The MOSFET's drain is also connected to a VR_RDY signal, which is connected to a 3D3V_AUX_S5 voltage source. The VR_RDY signal is also connected to a 3D3V_S0 voltage source. The VR_RDY signal is connected to the ECRST# pin of the ALC299 CODEC. The ALC299 CODEC is also connected to the SPK-OUT-R-, SPK-OUT-R+, LINE2-L, LINE2-R, HPOUT-L/PORT-T-L, HPOUT-R/PORT-T-R, LINE1-L, LINE1-R, SENSE_A, SMDL-CLK, and DMIC-DATA pins.

[illegible]